Investigation on Five Phase Inverter

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Abstract

In this paper, Sinusoidal Pulse width modulation (SINE-PWM) and Space Vector Pulse width modulation (SVPWM) techniques are implemented in the five phase inverter. Space vector modulation is realized using min-max method. Both SINE-PWM and SVPWM techniques are tested in simulation and hardware set-up. Results are obtained satisfactorily and it confirms the features of both PWM techniques.

Keywords: Five phase inverter, SINE-PWM, SVPWM

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INTRODUCTION

Induction machines are the work horse of the industry. In the present scenario, fivephase machines are popular in comparison with the conventional three-phase one. Multiphase drives are possessing low torque ripple, reduces harmonic content and reduction in current rating of the inverter leg.

Preliminary investigation of an inverter fed five phase induction motor was initiated by Ward. E. E and Harer H. in 1969^[1]. Levi. E *et al.* reviewed the various aspects of multiphase induction motor drives. Despite the mass production of three phase motors with low cost, there has been an upsurge of interest in multiphase machines due to the following principal reasons^[2].

- 1. Improvement in efficiency due to the lower harmonic content in the field produced by multiphase machines.
- 2. Greater fault tolerance in the absence of one, two or three phases of supply.
- 3. Less susceptible than their three phase counterparts to time harmonic components in the excitation waveform.
- 4. Elaborate flux and torque control with reduced torque ripple due to the

availability of 32 space voltage vectors instead of eight vectors in three phase inverter fed induction motor drives^[3].

Hamid A. Toliyat implemented an indirect field oriented control including hysteresis type pulse width modulated current regulator. Also the author described the fault tolerant analysis of five phase drive with the loss of one, two or even three legs of inverter^[4]. C'esar Cataldo Scharlau et al. implemented a modified open loop V/f control method with the improvement in iron utilization and higher output torque through the imposition of an appropriate combination of the third harmonic and fundamental stator voltages^[5]. Libo Zheng et al. proposed a dual plane vector control of a five phase induction machine for the achievement of better iron utilization and higher torque density without the increase in size of the inverter^[6]. Martin Jones *et al.* developed modified current control scheme drives for multiphase experimentally, which provides the operating ability with a perfect sinusoidal and balanced system of five phase currents^[7]. Libo Zheng *et al.* proposed a novel Direct Torque Control scheme for a Sensor less five-phase Induction Motor Drive which eliminates low harmonic currents with the full utilization of DC voltage^[8].

K. N. Pavithran *et al.* studied the five phase inverter fed five phase induction motor and fabricated five phase induction motor for conducting research experiments. The authors established the satisfactory operation of five phase drive when fed from pulse width- modulated inverter^[9].

G.K. Singh investigated the technical economic viability of using a number of phases higher than three in induction motor. The author highlighted the advantages of five phase induction motor and its applications such as in nuclear power plants^[10].

Atif Iqbal accomplished flexible modeling and independent control of multi-phase multi machines fed from a single VSI. The model developed by the author is very flexible so that any control strategies can be implemented^[11]. Optimum performance achievement of five phase induction motor for weak and remote grid system was presented by Shaikh Moinoddin *et al.*^[12]. M. Rizwan Khan and Atif Iqbal designed improved estimator for an rotor position/speed of a vector controlled five phase induction motor drive^[13]. M. Rizwan Khan et al. implemented Model Reference Adaptive System (MRAS)-based sensor less control of vector controlled five phase induction machine with current control in the stationary reference frame. The experimental results obtained by the authors are identical with that of three phase induction machines^[14].

Ned Mohan *et al.* proposed a simple Space Vector Pulse width modulation (SVPWM) for VSI-fed AC Algorithm Motor Drives^[15]. The authors explained Space Vector PWM control of voltage source inverter and implemented using classical carrier-based approach. The space vector PWM is explained without use of any additional definitions such as sector calculation, hexagon of states and vector decomposition. In continuation of this SVPWM is implemented by using the above mentioned algorithm in five-phase inverter.



Fig. 1: Block Diagram for Five-Phase Inverter with R-Load.

Five-Phase Inverter

The block diagram of five-phase inverter is shown in Figure 1. Here, five phase inverter is controlled by PWM techniques. Circuit diagram for five phase inverter with resistive load is shown in Figure 2. The five-phase inverter legs a, b, c, d, e are having one upper and one bottom switch. The switch status is S_a , S_b , S_c , S_d , S_e . If S_a is '1' means it represents upper switch, if it is '0' means it represents bottom switch. Output phase voltage waveform for five phase inverter under 180° mode of operation is shown in Figure 3. It clearly indicates the phase shift between each phase is 72° .



Fig. 2: Circuit Diagram of Five-Phase Voltage Source Inverter.



Fig. 3: 180° Mode Operation.

From the Figure 3, it is confirmed that peak value of the phase voltage is 60 V and the phase voltages are balanced.

Space Vector Pulse Width Modulation (SVPWM)

Space Vector Pulse Width Modulation (SVPWM) is one of the preferred real time modulation techniques and is widely used for digital control of Voltage Source Inverters. The SVPWM operates on the principle of 'Volt-second balance' which states that, product of voltage and second for the positive half cycle should be equal to the product of voltage and second for the negative half cycle. By simple digital calculation of the switching time one can easily implement the SVPWM scheme. Space vector diagram for five phase inverter is shown in Figure 4. It consists of 2^5 states.



Fig. 4: Space Vector diagram for Five-Phase Inverter.

In order to avoid the sector identification, the SVPWM is implemented by using Min-Max method. The main advantages of Min-Max method are Implementation of SVPWM without using Space vectors.



Fig. 5: Waveform of Five-Phase Supply for Min-Max Method of SVPWM.

In SVPWM each reference voltages are obtained from comparison of SINE wave and a triangular carrier. Common mode voltage is added in order to achieve maximum conceivable peak amplitude of the fundamental phase voltage^[15] with the reference phase voltage,

$$V_{\text{offset}} = - (V_{\text{max}} + V_{\text{min}})/2 \quad \text{Eq. (1)}$$

Where,

 V_{offset} = Common mode voltage

V_{max} = maximum magnitude of the three sampled reference phase voltages V_{min} = minimum magnitude of the three sampled reference phase voltages

The equation is based on the reference phase which has lowest magnitude (minphase) crosses the triangular carrier first and cause the first transition in the inverter switching state. Once the first-cross and fifth crossed are determined, the offset voltage is calculated from the equation mentioned above. The time instants at which the three reference phases cross the triangular are determined.

Sinusoidal Pulse Width Modulation (SINE-PWM)

SINE-PWM is one of the conventional control techniques for inverter. In this SINE-PWM, SINE wave is compared with a carrier triangular wave which will generate the PWM pulses for the inverter devices. SINE-PWM pulses can be varied by changing the modulation index value. In SINE-PWM there is no need for sector calculation, hexagon states and vector decomposition. This is a simplest PWM technique.



RESULTS

In order to compare SINE-PWM and SVPWM in five-phase inverter with resistive load, simulation and experimental

study are completed with the specification mentioned in Table 1. Simulation is done using MATLAB (Matrix Laboratory)^[13].

S.No	Parameters	Values
1	Switching Frequency (fs)	1 kHz
2	Device	MOSFET
3	PWM Technique	SINE-PWM
		SVPWM
4	Resistance	150 Ω
5	Input dc voltage(v)	100 V

Table 1: Specification of Five-Phase Inverter.

Simulation

Simulation results of SVPWM and SINE-PWM are shown in Figure 5 and Figure 6. Total harmonic distortion (THD) for the modulation techniques are presented in Figure 7.

From the Figure 5, it is seen that the peak value of the phase voltage is 80 V and the phase voltages are balanced. The pulse pattern and the corresponding phase voltages for SINE-PWM, for the switching frequency, $f_s = 1$ kHz are shown in Figure 6.

From this Figure it is inferred that, the peak value of the phase voltage is 66 V and the phase voltages are balanced.



Fig. 5: Simulation Results for Phase Voltages of SVPWM Inverter.



Fig. 6: Simulation Results for Phase Voltages of SINE-PWM Inverter.



Fig. 7(a): THD for SVPWM.



Fig. 7(b): THD for SINE-PWM.

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Comparison of SINE-PWM and SVPWM for five-phase inverter with R-load is completed based on the THD values in the output voltage of inverter with R-load. From the THD graph 7, it can be concluded that SINE-PWM will produces less amount of harmonics in comparison with SVPWM. This is due to the maintenance of half wave symmetry in SINE-PWM in comparison with SVPWM.

Hardware Implementation

The experimental setup for Five-phase inverter with R-load is shown in Figure 8.

100 V DC supply is given to the Fivephase inverter with R-Load of 100 Ω . Here for different modulation index the phase and were varied with SINE-PWM & SVPWM and THD value obtained using YOKOGAWA-WT 180. For increase in modulation index the output voltage value will increase.

The hardware results of SVPWM phase and line voltages for different modulation index and the PWM pulses for each device are completed and Figure 9–26 represents the results for modulation index 0.7.



Fig. 8: Five-Phase Inverter with Resistive Load Hardware Setup.



Fig. 9: Hardware Results of Pulses for a-Phase and b-Phase.



Fig. 10: Hardware Results of Pulses for c-Phase and d-Phase.



Fig. 11: Hardware Results of Pulses for e-Phase.



Fig. 12: Hardware Result of Phase Voltages Waveform of SVPWM.

From the Figure 12, it is seen that all the phase voltages are balanced and having peak voltage of 53V.



Fig. 13: Voltage and Current Values for Each Phases of SVPWM.

From the figure 13, it is confirmed that, Root mean Square (RMS) value of the phase voltages are same for all the phases. The Peak voltage for all the phases is unbalanced in hardware results, because the device drop for each device is different i.e., device mismatch.

Normal Mode	(Trg)	Peak O	/er Sc	aling 📒 L	ine Filter	Time Int	eg: Reset	PLL1: 10 50.232 Hz
_		11.1)11.2[11.3]11.4[11.3	AV	6 1	req Filter	x		PLL2:11 50.231 Hz
		Order	U1 [V]	hdf[%]	Order	U1 [V]	hdf[%]	Element 1 HRH1
fPLL1:U	50.232 Hz	Total	28.273		dc	0.052	0.186	U1 30V
fPLL2:1	50.231 Hz	1	26.044	92.118	2	0.326	1.155	Sync Srct 11
		3	0.121	0.427	4	0.134	0.475	Element 2 Here
Urms1	37.321 V	5	0.069	0.244	6	0.112	0.395	
Irms1	0.2422 A	7	0.084	0.297	8	0.294	1.040	I2 1A
P1	9.037 ₩	9	0.119	0.421	10	0.051	0.180	
S1	9.037 VA	11	0.097	0.344	12	0.255	0.903	Element 3 HRH1
Q1	0.106 var	13	0.151	0.535	14	0.049	0.173	13 1A
λ1	0.9999	15	0.143	0.507	16	0.102	0.362	Sync Src:
Φ1	G0.67 °	17	0.350	1.236	18	0.196	0.692	Element 4 HRM1
		19	0.148	0.522	20	0.135	0.478	<u>1 14 307</u>
Uthd1	38.914 %	21	0.098	0.347	22	0.677	2.395	Sync Src:
I thd1	38.826 %	23	2.556	9.039	24	0.397	1.405	Element 5 HEN1
Pthd1	15.108 %	25	2.323	8.218	26	0.786	2.781	U5 30V
Uthf1	38.965 %	27	1.253	4.432	28	0.763	2.698	15 5A
Ithf1	38.806 %	29	0.043	0.152	30	0.635	2.245	Sync Src. 10
Utif1	0 F	31	1.042	3.686	32	0.527	1.864	Element 6 Hight
ltif1	0 F	33	2.387	8.442	34	0.193	0.684	16 5A
hvf1	4.808 %	35	2.578	9.117	36	0.526	1.861	Sync Src: 📧
hcf1	4.788 %	37	0.073	0.257	38	0.198	0.702	
Kfact1	3.2265 k	39	0.165	0.585	40	0.079	0.279	
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Fig. 14: THD Values for a-Phase of SVPWM. From the Figure 14 THD value of Phase voltage is obtained as 38.914%.



Fig. 15: Line Voltages Waveform of SVPWM.

Figure 15 shows that, the line voltages are balanced and its peak voltage is 71 V.

Normal Mode(Tr	g)	Peak Ov Intra terretaria	er Scali AVG	ng Line F Freq F	ilter Time	nteg: Reset ::	YOKOGAWA PLL1: 01 50.232 Hz PLL2: 10 50.231 Hz
Voltage	Element 1 30V	Element 2	Element 3	Element 4	Element 5	Element 6	Element 1 HRM1
Urms [V]	37.321	37.110	37.231	37.219 0.2389	37.254	0.915 2	1 1A Sync Src:11
P [W] S [VA]	9.037	8.829	8.852	8.89	8.93 8.93	-0.00 3	U2 30V 12 1A
Q [var] λ []	0.106 0.9999	0.109 0.9999	0.200 0.9997	-0.22 0.9997	0.26 0.9996	0.00 4 Error	Element 3 HIBHT
◆ [°] 10 [Hz]	G0.67 50.232	G0.70 50.232	G1.30	D1.41	G1.65	Error 6	I3 1A Sync Src: IS
Urms [V]	37.321	37.110	37.231	37.219	37.254	0.915	U4 30V 14 5A Sync Src:E2
Umn [V] Udc [V]	31.532 0.034	31.378	31.466 -0.212	31.444 0.258	31.455 0.374	0.800 8	Element 5 HRH1
Uac [V] U+pk [V]	37.321	37.109	37.231	37.218	37.252	0.915 10	Sync Src:115 Element 6 HIBH1
U-pk [V] CrU []	-79.610 2.136	-79.624 2.146	-79.880 2.145	-80.362 2.159	-79.797 2.146	-2.706 11 2.996 12	U6 30V 16 5A Sync Src:10
Pc [#] P+pk [#] P-pk [#]	7.528 41.367 -0.096	7.361 40.708 -0.101	7.377 40.809 -0.307	7.40 45.23 -0.30	7.43 45.38 -0.07	-0.00 0.07	
Update 11	(500msec)	.8	0.001			201	3/05/07 16:16:35

Fig. 16: Voltage and Current Values for SVPWM for M=0.

From the Figure 16, it is found that the RMS value of the line voltage, 50.270 V. The Peak voltage for all the line voltages is unbalanced in hardware results which is

due to the difference in the device drop for each device.

Normal Mode(Trg)	Peak Ove	r Sci AV	aling L G F	ine Filter req Filter	Int Time	eg: Reset :	•: YOKOGAWA PLL1:01 50.231 Hz PLL2:01 50.232 Hz
	Order	U1 [V]	hdf[%]	Order	U1 [V]	hdf [%]	CF:3 Element 1 HIBH1
fPLL1:U1 50.231 Hz	Total	34.396		dc	0.269	0.781	U1 60V
fPLL2:11 50.232 Hz	1	29.766	86.539	2	0.084	0.243	Sync Src: 11
	3	0.039	0.112	4	0.138	0.401	Element 2 HEHI
Urms1 50.270 V	5	0.147	0.426	6	0.098	0.285	U2 60V
Irms1 0.2375 A	7	0.112	0.325	8	0.250	0.728	12 1A
P1 8.219 W	9	0.141	0.411	10	0.069	0.201	Sync Src. 12
S1 11.940 VA	11	0.186	0.541	12	0.172	0.500	Element 3 HBH1
Q1 -8.660 va	13	0.019	0.057	14	0.318	0.926	13 1A
λ1 0.6884	15	0.166	0.481	16	0.460	1.337	Sync Src: 13
Φ1 D46.50 °	17	0.644	1.872	18	0.468	1.360	Element 4 BRH1
	19	0.063	0.183	20	0.226	0.657	U4 60V
Uthd1 50.103 %	21	0.167	0.486	22	0.814	2.365	Sync Src: Ed
lthd1 38.052 %	23	2.738	7.960	24	0.125	0.364	Element 5 Mart
Pthd1 25.059 %	25	3.008	8.744	26	0.656	1.906	
Uthf1 40.413 %	27	2.307	6.708	28	0.901	2.621	15 5A
lthf1 37.627 %	29	0.071	0.206	30	0.668	1.943	Sync Src: 10
Utif10 F	31	1.961	5.700	32	1.120	3.257	Element 6 HRH1
Itif10 F	33	2.950	8.576	34	0.053	0.155	16 5A
hvf1 5.342 %	35	2.656	7.721	36	0.733	2.132	Sync Src: 13
hcf1 4.626 %	37	0.125	0.365	38	0.064	0.187	
Kfact1 3.2015 k	39	0.081	0.237	40	0.179	0.522	
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Fig. 10: THD Values for Line Voltage of SVPWM for M=0.7.

Figure 17 shows the THD value of Phase voltage with SVPWM is 50.103%. Hardware results of SINE-PWM phase and

line voltages for different modulation index and the PWM pulses for each device are shown in Figure 18–26.





Fig. 18: Hardware Results of Pulses for a-Phase and b-Phase.

Fig. 19: Hardware Results of Pulses for c-Phase and d-Phase.



Fig. 20: Hardware Results of Pulses for e-Phase.



Fig. 21: Phase Voltages Waveform with SINE-PWM.

Normal Mode(T	rg)	Peak Ov Intro2 Institution Intro2 Institution	er 100 Scali 100 AVG	ng Line Fi Freq Fi	lter <mark>–</mark> Time Iter –	Integ: Reset :	YOKOGAWA PLL1: U1 50.232 Hz PLL2: L1 50.233 Hz
Voltage Current	Element 1 30V 1A	Element 2 30V 1A	Element 3 30V 1A	Element 4 30V 5A	Element 5 30V 5A	Element 6	CF:3 Element 1 HRM1 U1 30V
Urms[V] Irms[A] P[W]	34.713 0.2251 7.813	34.540 0.2213 7.645	34.629 0.2217 7.676	34.627 0.2222 7.69	34.676 0.2231 7.73	0.930 0.0000 -0.00	L1 1A Sync Src: L1 Element 2 0000 U2 30V
S [VA] Q [var] λ []	7.813 0.098 0.9999	7.645 0.099 0.9999	7.678 0.182 0.9997	7.69 -0.20 0.9997	7.74 0.23 0.9995	0.00 0.00 Error	12 1A Sync Src: 12 Element 3 18841
∲ [°] ¶U [Hz] fl [Hz]	60.72 50.232 50.233	G0.74 50.232	G1.36	D1.49	G1.74	Error 5	I3 1A Sync Src: 18 Element 4 HRM1
Urms [V] Umn [V] Ude [V]	34.713 27.877	34.540 27.747	34.629 27.806	34.627 27.806	34.676 27.805	0.930 0.832 0.001	04 30V 14 5A Sync Src: 12 Element 5 H8M1
Urmn [V] Uac [V] Uac [V]	25.099 34.713 78.128	24.981 34.540 78.039	25.034 34.628 78.155	25.034 34.626 78.295	25.033 34.674 78.549	0.749 0.930 2.648	US 30V 15 5A Sync Src:15 Element 6 HRM1
U-pk [V] CfU [] Pc [W]	-78.042 2.251 6.127	-78.172 2.263 5.997	-78.238 2.259 6.018	-78.327 2.262 6.03	-78.380	$ \begin{array}{r} \hline 2.010 \\ -2.634 \\ 2.848 \\ -0.00 \\ 12 $	U6 30V 16 5A Sync Src:
P+pk [W] P-pk [W]	39.658 -0.153	39.238 -0.287	39.339 -0.294	42.61 -0.19	43.74 -0.11	0.06	
Update 2	(500msec)	.8				201	3/05/07 16:12:17

Fig. 22: Voltage and Current Values for SINE-PWM.

Normal Mode	e(Trg)	Peak O In 12 traina ta 11 12 traina ta	ver Fille Sc Gille Av	aling L 'G - F	ine Filter req Filter	Time	eg: Reset :	YOKOGAWA PLL1: U1 50.232 Hz PLL2: U1 50.233 Hz
4011.4.11		Order	U1 [V]	hdf[%]	Order	U1 [V]	hdf[%]	CF:3 Element 1 H8H1 U1 30V
€PLL1+U	1 50.232 HZ	1004	24.988	99 664		-0.068	0.771	11 1A
II LL2- I	1 00.200 112		0 161	0 646	á	0.133	0.569	Sync Src:
Urmst	34 713 V	5	0 168	0.673	6	0.234	0.936	Element 2 HRH1
Irms1	0 2251 A	7	0.058	0.231	Ř	0 303	1 213	12 1A
P1	7.813 W	9	0.076	0.305	10	0.068	0.274	Sync Src: 12
S1	7.813 VA	11	0.108	0.430	12	0.062	0.249	Element 3 HRH1
01	0.098 var	13	0.114	0.458	14	0.232	0.927	U3 30V 13 1A
λ1	0.9999	15	0.079	0.315	16	0.126	0.504	Sync Src: 13
Φ1	G0.72 °	17	0.064	0.256	18	0.043	0.174	Element 4 HRH1
		19	0.168	0.672	20	0.018	0.072	U4 30V
Uthd1	37.595 %	21	0.214	0.856	22	0.084	0.335	Svnc Src:
l thd1	37.513 %	23	1.300	5.201	24	0.290	1.160	Elomont 5 URM
Pthd1	14.102 %	25	3.384	13.542	26	0.491	1.963	
Uthf1	39.382 %	27	0.416	1.666	28	0.928	3.715	15 5A
lthf1	39.238 %	29	0.164	0.658	30	0.445	1.781	Sync Src. 18
Utif1	0 F	31	0.549	2.197	32	0.529	2.116	Element 6 HRM1
ltif1	0 F	33	3.224	12.903	34	0.279	1.118	16 5A
hvf1	4.906 %	35	1.428	5.715	36	0.072	0.287	Sync Src: 16
hcf1	4.893 %	37	0.205	0.820	38	0.259	1.035	
Kfact1	2.7521 k	39	0.166	0.663	40	0.162	0.649	
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T 1 (T T 1	0	D1		0.01		

Fig. 23: THD Values for Phase-a of SINE-PWM for M=0.7.

Figure 24 reveals that the RMS value of the phase voltages are same for all the phases. The Peak voltage for all the phases is unbalanced in hardware results and it is due to the mismatch in the device drop. THD value of Phase voltage is 37.595% in Figure 25.



Fig. 24: Line Voltages Waveform of Sine-PWM.

Normal Mode(Tr	(g)	Peak Ov	er .			nteg: Reset	YOKOGAWA	
			Scali	Scaling Line Filter Time:: AVG Filter				
	Element 1	_Element 2_	_Element 3_	_Element 4_	_Element 5_	_Element 6_	CF:3	
Voltage	60V	60V	60V	60V	60V	30V	Liement I Hos	
Uses DV 1	47,000	47.052	47 700	47.004	40.455		1 1A	
	47.620	47.303	47.730	47.034	46.155	0.000	2 Sync Src:11	
	7 409	7 220	7 000	7 22	7 42	-0.00	Element 2	
	10,901	10.004	10,020	10.00	10.70	0.00	3 U2 60V 12 1A	
	7 040	7 707	7 740	7 70	7.00	0.00	Sync Src:	
V Lvarj	0.0977	-1.131	-1.140	0.000	0.0000		Element 3 🗷	
	0.0011	0.0002	0.0052	0.0003	0.0000	Error	5 U3 60V	
	D46.56	D46.51	D46.75	G46.62	G46.48	Error		
	50.231	50.232						
TI [HZ]	50.231						Element 4	
Users DV 1	47,000	47.052	47 700	47.004	40.455		14 5A	
Units [V]	47.020	47.355	47.730	47.034	40.100	0.955	Sync Src: 14	
Unin LV J	27.036	27.192	27.003	21.151	27.425	0.001	🛃 Element 5 📠	
	0.200	0.005	-0.354	-0.081	0.152	0.002	U 5 60V	
Urmin LV J	24.341	29.481	24.312	24.450	24.692	0.748	Sync Src:III	
Uac LV J	47.820	47.953	47.794	47.894	48.155	0.955		
U+pk [V]	100.279	99.208	100.851	101.918	100.623	2.813		
U-pk [V]	-100.527	-99.058	-99.244	-101.562	-100.947	-2.836	16 5A	
CTU L J	2.102	2.069	2.110	2.128	2.096	2.970	2 Sync Src: 10	
Pc [#]	3.598	3.571	3.527	3.57	3.64	-0.00		
P+pk [#]	50.037	49.548	49.568	54.96	55.37	0.07		
P-pk [#]	-7.471	-7.244	-8.819	-7.47	-7.30	-0.08		
Jødate 1	(500msec)	.8				20	013/05/07 15:57:0	

Fig. 25: Voltage and Current Values for Sine-PWM.

Normal Mode	(Irg)		Peak Uv	/er So	aling 🗾 I	ine Eilter	Time Int	eg: Reset	
				AV AV	G i	Freq Filter			PLL2: 11 50.231 Hz
									CF:3
	F 0 0 1		Order		hdf[%]	Order		hdf[%]	Element 1 Hiert
TPLL1:U	50.231	HZ	Total	30.692	00.000	dC	0.083	0.270	11 1A
TPLL2:1	1 50.231	HZ	1 1	27.077	88.222	2	0.134	0.437	Sync Src: 11
	17.000		1 ³	0.257	0.838	1	0.199	0.648	Element 2 Hight
Urms1	47.820	v	5	0.107	0.350	6	0.374	1.219	U2 60V
Trins1	0.2259	Α		0.106	0.346	8	0.307	1.000	Sync Src:12
P1	7.428	W	9	0.175	0.569	10	0.125	0.406	Element 2
S1	10.801	VA	11	0.084	0.274	12	0.063	0.205	
Q1	-7.842	var	13	0.102	0.333	14	0.184	0.601	13 <u>1A</u>
λ1	0.6877		15	0.165	0.538	16	0.083	0.269	Sync Src: 18
Ф1	D46.56	•	17	0.164	0.534	18	0.031	0.102	Element 4 HEM1
			19	0.055	0.178	20	0.189	0.616	14 5A
Uthd1	47.082	%	21	0.513	1.672	22	0.038	0.124	Sync Src:
I thd1	36.789	%	23	1.448	4.717	24	0.025	0.083	Element 5 HRM1
Pthd1	21.714	%	25	4.008	13.059	26	0.908	2.957	US 60V
Uthf1	41.472	%	27	0.786	2.562	28	0.912	2.971	15 5A Sumo Scotter
Ithf1	38.822	%	29	0.097	0.316	30	0.777	2.533	
Utif1	0 F		31	0.697	2.270	32	1.054	3.435	Liement 6 Hight
ltif1	0 F		33	3.906	12.728	34	0.169	0.552	16 5A
hvf1	5.333	%	35	1.501	4.890	36	0.034	0.109	Sync Src: 10
hcf1	4.800	%	37	0.374	1.219	38	0.278	0.907	
Kfact1	2.6712	k	39	0.089	0.291	40	0.138	0.448	
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Fig. 26: THD Values for Line Voltage of Sine-PWM.

From the Figure 26, THD value of Phase voltage is found to be 47.082%. Table 2 shows the comparison between SINE-PWM and SVPWM. From the table, it can

be confirmed that, SINE-PWM performs better than SVPWM due to the maintenance in symmetry.

Modulation Index, M	0.5	0.7	0.8
SVPWM	49.382	38.914	39.773
SINE-PWM	29.126	37.595	39.19

 Table 2: THD Comparison of SINE-PWM and SVPWM.

CONCLUSION

This paper has explained the five-phase inverter operation for both r-load with 180° mode of operation, SINE-PWM, and SVPWM. Basic operation of five-phase inverter is theoretically studied and simulated. Further, performance of SINE-PWM and SVPWM are compared in simulation and hardware for five-phase inverter with r-load. From the results, it can be concluded that THD for SINE-PWM is lesser in comparison with SVPWM. Investigation of five phase inverter fed induction machine is in progress.

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