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Integration of Electronic Devices and the Current Applied MOS Techniques

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Abstract

This is a research based review of the comprehensive view of our understandings for VLSI which is evolved from integrated circuits with a numbers of transistors ranging from several billions of devices which also include chip and sensors. The VLSI concept based design and implementation are categorized accordingly. It deals with architectural factors, which also describe these for both general-purpose and digital systems and their coexistence with analog, mixed-signal and radio frequency components as used in many applications nowadays. The standard of circuit design, have impacts like complexity, power, digital-analog coexistence, and more. Due to this, the evolution of MOS technologies are possible and a single glimpse on sensing devices compatible with MOS offer flavors of future combining MOS and sensors. Lastly, we have several different auxiliary techniques required to design and implement VLSI.

Keywords: *Very large scale integration, mean opinion score, analogue integrated circuits*

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INTRODUCTION

The concept of very large scale integration was coined for describing the process of designing and fabricating integrated circuits and combining number of transistors and their interconnections in a chip. This happens when the mean opinion score technologies have size larger than 1 nm. As technology evolved towards smaller sizes, decreasing more, the term VLSI applied to chips, forms thousands and even millions of transistors. Hence, the minimum dimensions have been shrinking down to billions of transistors [1]. Historically, the first integrated circuits consisted only of a few components, making it possible to fabricate one or more logic gates on a single device, in what is now retrospectively known as small-scale integration (SSI). Afterwards, further improvements in technology led to chips with hundreds of logic gates, the so-called medium-scale integration (MSI), and even more than thousand logic gates (large-scale integration or LSI). Then, it comes up the definition of VLSI attached to integrated circuits approaching one hundred thousand devices. In the past, as current technology moves far away these numbers, there was an effort to name and define other levels of large-scale integration, like ultra-large-scale integration (ULSI); but this trial was abandoned due to the fast pace in reducing sizes and increasing complexity; and the volatility of any definition. An empirical law, the well-known "Moore Law" [2], states that the density of transistor in a chip doubles approximately every 18 months.

Thus, present MOS technologies provide chips with many billions of transistors and there is no forecast on the limits to be reached as current generation processes move from 65 and 45 nm to generations in the proximity of 10 nm and beyond. This continuous movement towards smaller

dimensions is what nowadays is known as "More Moore" tendency in the evolution of integration, as it is foreseen that there is still room to continue with the reduction of dimensions for the next decade or so. In this sense, we can define a coordinate which has been primarily determining the different generations of VLSI circuits, namely the device dimensions. Vertical axis is indicating how size has been shrunk.

The upper clouds indicate which have been the baseline circuits (microprocessors and memories) and the one to the left indicates that probably after reaching the scaling limits for CMOS, this evolution will continue supported by new devices beyond CMOS. It is due to the need of incorporating non-digital devices into a chip since new application fields are demanding the usage of analog circuits, sensors and/or actuators within the same semiconductor substrate. This requires several changes in the design flow of complex ICs and poses as well new problems to be solved. An overview of this emerging tendency can be seen from non-digital devices, like analog and RF components, passive elements, power transistors, sensors, actuators and even devices which can be considered beyond traditional paradigms as biochips, fall into this new category. Systems included there are not as well-defined as their opportunity is driven by market needs combining to technological feasibility. Finally, there is a third coordinate that, although tightly related to the More-than-Moore concept, worth considering as a separate entity. It is the incorporation of heterogeneity into integrated systems. In that sense, there are two already coined names to include the cases under focus nowadays: System-on-Chip (SoC) and System-in-Package (SiP); where both concepts are represented. In fact, SoC is a general name for systems including any class of devices on a common semiconductor substrate. When this is the case, interactions with the external world are only done in the actual periphery of the system, avoiding perturbations due to interconnect with the own system components. Of course, there are other problems caused by the common substrate, and they need to be adequately circumvented. Similarly, SiP corresponds to systems where components can be fabricated in the most convenient technology as they are finally assembled in a way that reduces the interactions with the external environment.

Then, the term VLSI has no longer just a meaning related to the number of transistors but to the complexity a chip may have. Any integrated circuits including either or both; (a) a huge number of digital devices, (b) many digital and non-digital devices (analog, RF, sensors, actuators) are considered VLSI as they are hard to design and put on the foreground many usual requirements to be taken into account when these chips have to be designed, fabricated and tested. Besides that, these systems can be realized or not on the same semiconductor substrate, giving a high flexibility in terms of market acceptance.

In this sense, we can admit as an updated definition of the term the following: VLSI is a term associated with the integration of dense and complex chips forming a system, without a precise quantitative measure of any of these two properties (density and complexity); these systems can be realized on the same semiconductor substrate or combining different ones but connected by semiconducting wires. Then, the three coordinates previously introduced combine into a design space as shown in Figure 1, which is the space in which any modern-days VLSI must exist.

VLSI DESIGN SPACE

Although the vision may induce the idea that we are handling three coordinates we can deal independently with, this is not true. In fact, that figure is just a conceptual

high-level view of the problem. Actually, interactions among the three coordinates are very strong, making difficult even a clear separation. As has been mentioned, a more realistic vision can be obtained from Figure 1, where the VLSI design space is represented as two-dimensional since SoC or SiP are tackled when higher-value systems are the target. In Figure 1, it should be clear that there are a number of significant topics having a key influence on the efficiency of modern VLSI circuits.

1. Advanced MOS technologies.
2. Deep submicron design and modeling issues, including methods to handle process variations through the incorporation of statistical design techniques.
3. Logic and high-level synthesis.
4. Digital systems and architectures.
5. Digital signal processing and image processing IC design.
6. Analog, mixed-signal (MS) and radio frequency (RF) IC design.
7. Testability and design for test.
8. CAD tools, from specialized design tools to design frames, including design flows.
9. Interconnects, 3-D integration and physical design.
10. Low-power and thermal-aware design, including power management and methods to reduce dynamic power dissipation in scaled technologies, like dynamic bias or frequency scaling.
11. Timing and clocking issues: clock generation and distribution, time verification, clock skew, asynchronous techniques.
12. SoC design: non-electrical model, MOS-compatible micro sensors.
13. New architectures and compilers, reconfigurable systems.
14. Prototyping, validation, verification, modeling and simulation.
15. Embedded systems design, hardware-software co-design and real-time systems.

When globally considering its evolution along years, we can state that, since the times when the VLSI term was introduced, there have been a lot of changes conditioning the important issues having influence. First of all, the evolution of technology, which has shrunk down below barriers not even envisioned in those first times. This evolution translated into a higher number of devices per chip, in accordance to Moore's law. However, this has also influenced other design constraints. One of them is power density. As devices are going smaller, power density has increased several orders of magnitude, requiring new methods to dissipate the heat. Related to dimensions as well, there is an ever increasing problem: reliability is severely affected due to dimension reduction combined with power dissipation. The fact is a decrease on reliability. Another impact of technology evolution is the need to cope with parameters affected by larger random variations, thus forcing the designer to use more and more statistical design tools and incorporating more complex models for transistors and connections. So, most circuit properties are correlated, techniques at different abstraction level must be considered for increasing power dissipation.

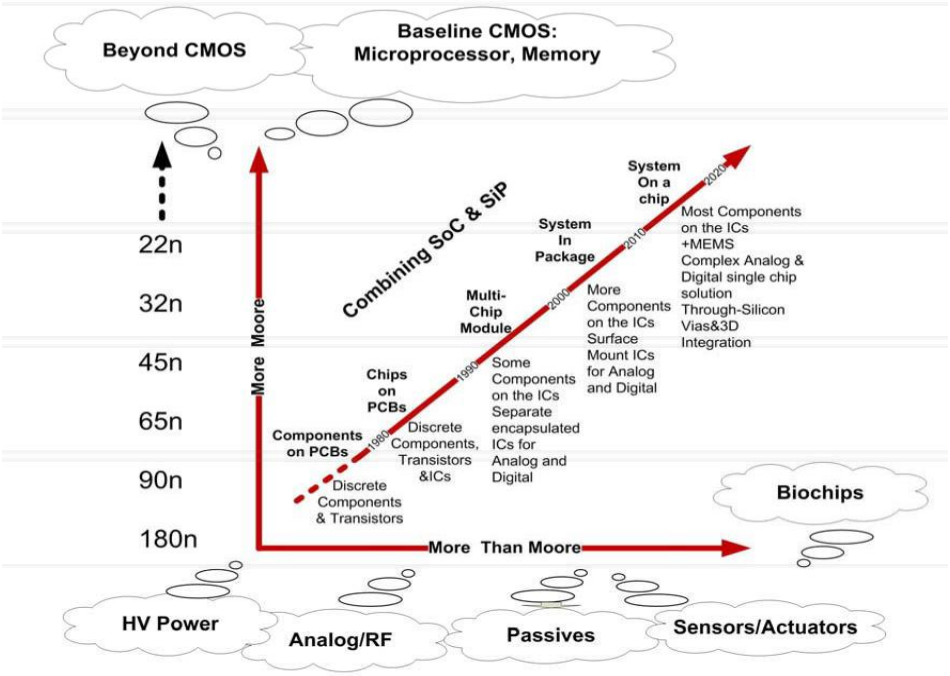

Fig. 1: *VLSI Design Space.*

For instance, increasing speed requires increasing bias voltages, which also increases power dissipation. A popular technique at system-level is to benefit of the maximum speed only where and when is really needed. To do that, several bias voltages are used instead of a single value. Then, higher bias will be used for high-speed, high-power parts and lower supplies for those parts where energy has to be saved.

Coexistence of AD Components

Coexistence of analog and digital components on the same semiconductor substrate also poses new problems. A common substrate facilitates undesired interactions between both kinds of components. Digital noise is spread all over the chip and may cause troubles during the operation of analog circuitry [3–20]. Methods to reduce substrate coupling or to isolate the analog parts are essential for the operation of complex VLSI nowadays.

Interconnection is another important issue. The number of external pins is very limited for modern VLSI chips, what means a reduced mechanism for interaction with the external world. The consequences are twofold. First, most pins are reserved for biasing, grounding, and continuous time signals, being quite a few the number of digital access ports. A second consequence, related to the previous one, is that testing is becoming cumbersome. Testing digital devices is more and more difficult due to the restricted pin numbers [4, 21–26]. Moreover, a real-life testing implies the simultaneous at-speed testing of analog and digital subsystems. This is particularly difficult due to the ad-hoc nature of analog test as well as to the lack of enough access terminals to readout the test signals outputs. Specific tests for such complex systems are under study [5]. For digital circuitry, there exist general test techniques since long ago, which can be considered adequate. However, for such complex digital systems, there is not always possible to find efficient solutions. Today digital fault models, for advanced technologies, are complex and are not so well-established as they used to be in the past. Traditional fault models like stuck-at models are not reflecting the kind of faults one may find in modern MOS

technologies. Even more, failure mechanisms as those affecting micro-sensors (or nanosensors) are far from being satisfactorily modeled at an electrical level. New interconnects are then under development, like 3-D integration, which addresses the construction of SiP as an alternative to complex SoC. This idea is based on mounting together (one on top of another) two or even more chips, connecting them through silicon vias. The gain is a higher density as well as the advantages of using different MOS technologies for every chip. However, power dissipation may be still a problem as well as semiconductor vias are not yet mature.

Timing is also an issue. For large chips, efficient clock distribution is quite a formidable task [6]. For totally-synchronous designs there are problems related to clock skew, clock power consumption, clock distribution along the chip, fan-out, etc. And this is even more complex when there are mixed-signal components, which usually also require a clock. Asynchronous or partially-synchronous techniques are beginning to be popular, although their disadvantages are not always compensated by their advantages. Besides the fact that a synchronism may avoid problems related to the clocking itself, this also reduces power dissipation, since the chip activity is restricted to the processing events. In other words, instead of a periodic activity controlled by the clock, circuit parts which are not operative can be asleep. Even mixed-signal circuitry (basically, data converters) are now targeting the use of a non-synchronous paradigm [25–36].

As far as sensors and actuators are incorporating to VLSI, there are other difficulties related to technology and its modeling. Sensors and actuators may require non-electrical models which have to be compatible with the regular design flow, based on electrical simulators. Both, the incorporation of these extended models and the design flow extensions or modifications, must be targeted in modern days VLSI research.

Talking about design flows, the incorporation of non-digital devices forces to much more complex flows, where compatibility between components is essential. In addition, verification issues are more and more needed since guaranteeing a first-silicon working is not an easy task. Design flows and their associated tasks are supported by CAD (Computer Aided Design) tools, which are also becoming more complex and since long ago are integrated in the so-called design frameworks and platforms. The number and diversity of tools to be used are dependent on the particular chip to be realized [37–50].

CONCLUSION

Architectural issues need also to be adapted to manage with efficiency non-digital subsystems. Nevertheless, all the topics need to be revisited since complexity increasing has an impact on them, and they need to coexist with More-than-Moore devices with which digital circuitry have to cooperate within the chip. Most topics listed above can be further grouped into categories related to the abstraction level from which a VLSI circuit is contemplated. In this sense, we can consider three basic ones, starting from the more abstract to the more physical:

a. Architectural,
b. Circuit design,
c. Technology-related.

Every category will be reviewed with the aim of offering the flavor of role within the VLSI system creation. Although some of these categories may have connections to more than one abstraction level.

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