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Analog Radio Frequency Circuits Design Technologies in Nanoscale Integrated Circuits

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Abstract

The evolution of the complementary nanoscale metal oxide semi-conductors has resulted in many analog design issues. Gate-leakage mismatches exceeded tolerances that require active and alternative cancelation techniques and architectures that give rise to techniques of low voltage. Therefore, functionalities are shifted to the digital domains that also include parts and imperfections of both analog and digital radio frequency circuits.

Keywords: *Digital control, radio frequency circuits, analog circuits, design issues*

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INTRODUCTION

Everywhere in our society, electronic systems have emerged. In terms of their (added) functionality, they are very cheap and sometimes even just become fashion items such as mobile phones and MP3 players. The key to low-cost systems is mass production using integrated circuits. Board design is made easier thanks to integration, and systems can be produced at low cost with the right software. Highly digitized today's systems allow this integration into CMOS technology.

The evolution in CMOS technology is motivated by decreasing price-per-performance for digital circuitry; its pace is determined by Moore's law. To ensure sufficient lifetime for digital circuitry and to keep power consumption at an acceptable level, the dimension-shrink is accompanied by lowering of nominal supply voltages. While this evolution in CMOS technology is by definition very beneficial for digital circuits, this is not so for analog circuits[1–3].

Contemporary ICs are mixed-signal systems consisting of a large digital core including a CPU or DSP and memory among others, often surrounded by multiple analog interface blocks such as I / O, D / A and A / D converters, RF front ends and more. All these functions would ideally be integrated on a single die from an integration point of view. The analog electronics must be realized on the same die as the digital core in this case and must therefore cope with the digital circuit dictated CMOS evolution.

To analyze the need from a circuit point of view, we first look at system trends and then look at the trends in CMOS technology. The circuit designer's task is to bridge the widening analog gap between system requirements and the CMOS technology available.

SYSTEMS

The system design trend is double. On the one hand, there is a trend towards integrating more functionality into a single multi-purpose device, including PCs, palmtop computers or mobile phones. These systems consist of a digital calculation core for general purpose with a reconfigurable user interface and a limited amount of dedicated I / O functionality. A multitude of different tasks can be performed using these systems. These tasks range from playing music, games,

movies, etc. to the bare functionality (e.g. making a phone call). It is easy to add functionality by adding software. Software is running in this first class of systems and digital signals are processed. Therefore, in advanced CMOS technology, the digital core of these systems is preferably manufactured to get low cost per computation and low power per computation at the same time.

On the other hand, there is a trend towards making more distributed, invisible electronic systems targeting data collection or delivery. These (user-friendly) invisible systems are generally used to control other systems and are therefore highly optimized for a specific task, such as sensing the oil pressure in a car or RFID. These systems can be viewed for a larger system as sensors or I / O devices. The core of this larger system is usually a multi-purpose programmable device: a first-class system. The sensory electronics contain dedicated sensors and hardware for communication and little intelligence; they can be produced in a technology that is optimized for these functions, which is not typically advanced CMOS due to cost reasons and the little need for a large digital core.

Analog in Systems

The real analog world needs to be interfaced by almost all systems. Because the signal processing is done primarily for efficiency reasons in the digital domain, the required AD converters and DA converters move to the edge of the system. At the same time, traditionally digital blocks like I / O are becoming increasingly analog because of either high-speed or high-voltage requirements. As with any analog circuit, the performance of the AD converter comes at the expense of area and power consumption. For this reason, putting analog preprocessing circuits such as amplifiers, filters and frequency translation circuits in front of the ADC remains beneficial to relax its performance requirements.

Researchers have been trying to integrate these circuits into CMOS technology since the 1970s, which is developed primarily for digital circuits. The resulting compact and low-cost single chip solution is the advantage of integrating analog with digital circuits. Integrated into CMOS during the eighties analog video baseband circuits covering the low frequency range of MHZ. Also RF circuits for the low GHz range could be designed in CMOS in the nineties because the technology's speed meanwhile became sufficient. While companies were reluctant to place RF circuits in CMOS, universities continued to investigate and develop new techniques. Today fully integrated RF transceivers can be produced on a single CMOS die [4–6], including digital baseband and MAC layers.

Maybe single chip CMOS transceivers aren't today's best-performing or most cost-effective solutions, but the problems are solved bit by bit due to a lot of research effort.

Analog Challenge from a System Point of View

The next challenge for the analog designers can be divided into two directions in a system point of view. The first is to use advances in technology and move to higher frequencies, such as communications with 60 GHz and radar. The second direction is to digitize the RF sections to make multiple RF standards more programmable and more flexible. This trend is towards, for example, radio software[7,8].

TECHNOLOGY ISSUES

Planar bulk CMOS has been scaled down to lower and lower dimensions in the last few decades of technology evolution, breaking forecast limits to scaling all the time. There is, however, consensus that

planar bulk CMOS scaling will stop around the 45 nm node in the near future. First, some issues related to more or less conventional CMOS are scaled down to the 45 nm node in this part of the paper; are addressed. A number of items related to the planar bulk device's successor will be reviewed later.

Output Conductance Effects

Transistor gain and its linearity aspects are one of the major issues in analog design. These improve with newer CMOS technologies, as shown by Annema et al., provided the headroom voltage and the length of the transistor are not scaled down[3]. This is illustrated in Figure 1: with newer technologies at constant transistor length L and constant voltage headroom, the gain and the IP3 do not change significantly. With lower headroom voltage, transistor performance decreases.

The transistor gain is less limited by digital circuitry requirements in ultra-deep sub-micron (UDSM) CMOS technologies. At least 10 voltage gains are required for its robustness using the minimum-length devices, which also results in the relatively weak relationship between output conductance and technology shown in Figure 1. However, the scaling of conventional planar bulk devices will stop due to the problems of getting enough (digital) gain below the 45 nm technology node. A discussion of the solutions envisaged will be presented in this paper later.

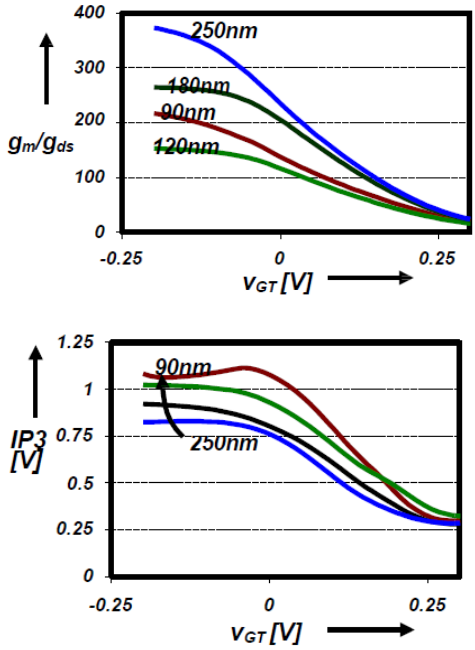

Fig. 1: *Various DC-Properties of Transistors as a Function of the Gate-Overdrive Voltage with VDS =0.3 V and L=1 um for Four Technologies:* ***(a)*** *the Gain, and* ***(b)*** *the Output IP3.*

Gate Leakage Effects

The significant gate-leakage is one of the relatively new effects in ultra-deep submicron CMOS. In low-frequency applications such as PLL-loopfilters and hold-circuits with long-term constants, one of the first areas where this became eminent. UDSM CMOS gate-leakage nowadays can be a serious problem in the design of analog circuits because: a. It poses lower limits for integrator circuits to the usable frequency range; e.g. for filters and hold circuits.

b. It introduces a strong relationship between the current DC gain and the length of the transistor, effectively limiting precision.
c. Its lack of match introduces a new level of accuracy that can be achieved.
d. Gate-current shot noise.

Using a MOS transistor fgate, all these effects can be easily estimated. For conventional MOS transistors, this area-independent and fairlyvDS-independent parameter is[3].

With newer technologies, however, the maximum hold time decreases rapidly, down to a typical value for standard 65 nm technologies in the low nano-second range. Either thick oxide transistors or inter-metal capacitances must be used to achieve an acceptable hold-time in 65 nm CMOS; similar conclusions hold for PLL loop filters.

Leaky gates result in DC-input current, which sets a lower limit to a MOS transistor's current gain; as a rough estimate, this DC gain is:

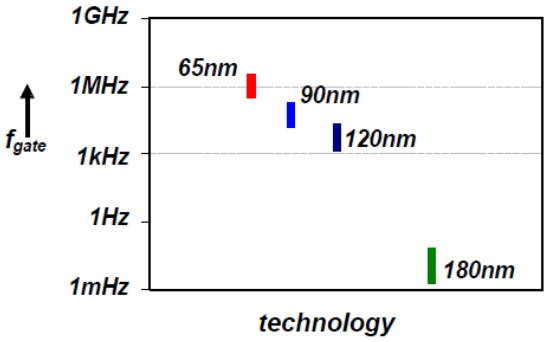

Fig. 2: *f_{gate} Ranges for Typical Analog Applications, for NMOS-Transistors in Different CMOS Technologies. For PMOS-Transistors f_{gate} is roughly a Factor 3 Lower.*

Figure 2 shows fgate-bands based on measurements for four technologies. This figure shows that fgate ranges from approximately 0.1 Hz in 180 nm technologies to approximately 1 MHz in 65 nm CMOS; fgate is approximately a factor 3 lower for PMOS transistors. This fgate can be used to estimate easily the impact of gate leakage on other relevant MOS transistor properties.

The Impact of Gate-Leakage on Matching

Quantum-mechanical tunneling causes gate leakage and depends on layer thickness and field strength. Therefore, it displays spread that can limit the analog circuit performance level that can be achieved. Since spread and mismatch are DC effects, they do not require any additional power (from a fundamental point of view). The typical way of minimization, however, is spending area, which in turn increases power consumption at a given speed[9,10] because it is necessary to charge larger capacitances[11].

A constant independent of area and (almost) independent of technology in this relationship. It directly follows those high gate values resulting in a large gate-leakage-related mismatch impact. The previous relationship also shows that the classical mismatch term decreases while at the same time the gate-leakage term increases by linear scaling of transistors (increasing the width and length proportionally), with constant power consumption. This results in a maximum usable area and a lower limit on achievable non-compliance. There is no minimum in the achievable mismatch figure with width-scaling and a proportional power-scaling. It is also evident that the gate has a significant impact on the minimum achievable mismatch figure: thus, low-

leakage devices should be used for maximum matching.

The fully depleted transistors are essentially thin-film SOI transistors that are present in many flavors. Figure 4b shows the type most similar in Figure 4a to the planar bulk device. The double-gate variant likely to be the successor or planar bulk devices is the FinFET[12–16] shown in Figures 4c and 4d. The name of the FinFET comes from its appearance (Figure 4d); the device resembles a silicon fin on top of a SiO2 layer, with the gate draped over it to form a gate on both sides of the gate (usually only) fin. Figure 3 shows the distribution of a 65 nm CMOS MOS transistor with a) linear scaling of W and L at constant power consumption b) W-scaling and proportional power scaling.

The Impact of Gate-Leakage on Noise

Gate leakage exhibits shot-noise with current density just like any current across a junction. As such, it is equivalent to bipolar transistor base currents. This noise of the shot comes over the induced noise of the gate[17,18]. Therefore, noise in the gate current limits noise performance in UDSM CMOS analog circuits[19].

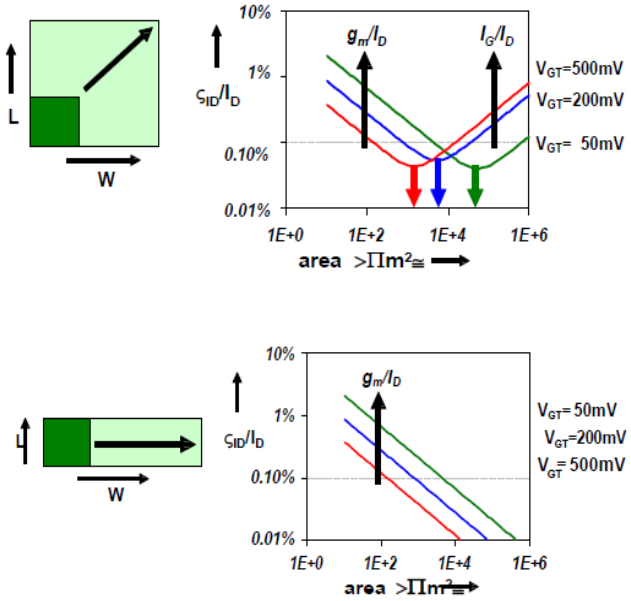

Fig. 3: *The Spread of an MOS Transistor in 65 nm CMOS with* ***(a)*** *Linear Scaling of W and L at Constant Power Consumption,* ***(b)*** *W-Scaling, and Proportional Power Scaling.*

FUTURE CMOS TRANSISTORS

The transistors in mainstream CMOS technology have been planar bulk devices over the past few decades. It is expected that scaling of these planar bulk devices will end around the 45 nm technology node[20,12]. The most likely successors are thin-body transistors that are fully depleted (FD)[12,21]. The advantages of these FD thin-body transistors over conventional UDSM transistors are several:

a. The body of the FinFET will be almost undoped, while the threshold voltage will be determined by the work function between the silicon and the metal gate[22]. As a result both gate depletion and threshold voltage, spread due to dopant number fluctuations in the body, are essentially absent.
b. The spread in the fin-width and the spread in the function[22] will determine Vt-spread. The expected mismatch and area-scaling relationships are not yet good data.
c. Conduction takes place on the sidewalls of the fin, which are formed by etching this surface is rough which

probably gives rise to excess flicker noise.

d. Due to reduced fields and quantum containment effects, the gate-leakage of FinFETs is reduced by about one order of magnitude compared to that of planar devices[23].
e. The mobility and therefore the current factor of the transistor is dependent on orientation in FinFETs due to the conduction on the sidewalls of the fine: the orientation of the crystal can be anything from (1 0 0) to (1 1 0) that significantly affects the mobility of the carrier[15,24]. It is expected that this orientation dependence will give no problems in analog circuit design as it is a good practice to layout in the same orientation matching sensitive transistors.
f. In SOI transistors, heat transfer is lower than in bulk devices: SiO2's thermal conductivity is about two orders of magnitude lower than Si's. This can result in transistor heating for typical analog applications with relatively low gate-source overdrive voltage and drain-source voltage. Heating results in shifted parameters of the transistor which can lead to effects of mismatch or thermal hysteresis [25, 26]. The temperature may have to be included as a state variable for precise analog models.

All together, the FinFETs have a number of parameters that are better than those of conventional devices: output conductance, gate-leakage and junction capacitances are lower. A number of new effects are introduced; most notably new mismatch effects, heating effects and flicker noise which introduce many unknowns in circuit design. With the current design aspects of UDSM CMOS technologies[3], this gives many new research opportunities.

CIRCUIT DESIGN CHALLENGES AND OPPORTUNITIES

Analog / RF moves from a system point of view to either higher speeds or higher flexibility, enabling the processing of software signals. Digital properties improve from a technology point of view, while at the same time the analog properties get worse. With this in mind it is possible to predict the role of analog circuits for the future. We propose to classify four types of electronic circuits for this purpose:

1. Digital pure circuits,
2. Digital analog circuit,
3. Digital circuits for analog,
4. Pure circuits of the analog.

Pure Digital Circuits

The complexity of pure digital circuits will continue to grow. Driven by the law of Moore, the number of gates will increase exponentially and the high gate count will be exploited by cost-effective ICs. Such complex ICs are difficult to monitor, and this is one of the reasons why digital ICs will contain multiple processor cores (or tiles), memory, and dedicated digital hardware. At locally high speeds and relatively slow networking over "large distances," the cores can operate in parallel[27]. Highly automated pure digital design work, and higher-order description languages such as VHDL are common practice today. It is very expensive to develop a complex IC in modern technology and therefore it is advantageous to use the same IC (hardware) in different applications by programming its software functionality. One of the big challenges is to program such a system efficiently as parallel processing is poorly supported by the programming languages of today.

Digital ways to increase the robustness of essentially digital systems include parity checks and ECC (error checking and correction) that are found primarily in memories and channels of communication [28].

Analog Circuits for Digital

Pure digital ICs contain some basic real analog functions such as power-on-reset and an internal high-speed low-jitter clock generation PLL that obviously copes with classical analog implementation issues. The "pure digital" circuits, however, face analog problems as well. Signal integrity[29] was one of the first problems encountered: digital switching itself creates bounce on supplies and substratum nodes in such a way that gate speed drops significantly and even functional errors result. These problems can be solved at the cost of area[29] by proper on-chip decoupling.

Digital ICs ' power consumption depends heavily on the supply voltage and the frequency of the clock. Adaptive supply voltages and clocks may be used to minimize power consumption. For this purpose, DC-DC converters can be used in control systems where both the frequency of the clock and the supply are reduced in such a way that the calculation is done just in time. This adaptive supply in practical ICs can result in significant power savings[30,31].

The addition of many analog circuits as sensors in large digital ICs is another application of emerging analog control for digital circuits. In doing so, the design does not need to take into account immunity to process variation and temperature margin, which can save considerable overhead and power consumption. Examples include measuring the local supply voltage[32], the local temperature[33], jitter etc. and adapting to them. Another application of sensory electronics in combination with actuators is the cancellation of unwanted disturbances [34].

The compatibility of new products with old ones is another issue related to the power supply of digital ICs. ICs ' internal supply voltage has dropped from 5 V to 1 V today over the past decade. The PCB board designs still use higher voltage swings and supplies as standards, though lagging behind them. Sometimes, therefore, the modern digital ICs should still look from the outside as if they are operating on a higher supply voltage than they are internally used. This is particularly the case with commodity products such as microcontrollers. For this reason, in modern CMOS technologies, fully integrated supply voltage regulators[35,36] and high voltage IO buffers[37] were developed. These circuits are designed at a voltage higher than nominal, but the circuits can withstand the high voltages by carefully stacking devices.

More attention is being paid to on-chip communication, as (global) interconnections for digital systems are rapidly becoming a bottleneck for speed, power and reliability[38]. Technological advances such as copper interconnections and low-k dielectrics are not enough to allow the interconnect bandwidth to match the transistor speed advances.

A general solution from a circuit-design perspective is the use of repeaters, which in terms of area and power is expensive. Another solution proposed uses low-swing signals over aluminum 10 mm differential interconnections[39]. Chang et al. suggested using 16 μm wide differential wires (20 mm long) and exploiting these wires ' LC (transmission line behavior) regime=[40].

Schinkel et al. demonstrated that pre-emphasisof pulse-width in combination with resistive termination can increase the data rate to 3 Gb / s / ch using differential interconnections of 10 mm long and 0.4 μm wide[41]. These interconnections can reach only 0.55 Gb / s / ch without the proposed techniques. Thus, a factor 6 in speed increase can be achieved over large distances by using analog equalizers that still conform to pure digital swing.

Typically, digital circuits for analog CMOS circuits reside on an IC with digital circuits for the processing of signals. Since digital circuits have become very compact, analog circuits can now be helped by digital circuits: the analog circuits can be calibrated and the non-ideal behavior can be corrected. While normal signals are processed or offline in a special calibration mode, this calibration can be done online. This correction can be done in turn in the analog domain (where a DA converter typically injects a static signal into the analog circuit) or in the digital domain (where an error can be removed). Below you will find some examples of calibrated circuits. This calibration trend can be clearly seen in AD converters. This makes it possible to use simple power-efficient open-loop residue amplifiers that are more compatible with modern CMOS technologies. With a calibrated auxiliary ADC, ADCs can even be calibrated online in the background. Wang et al. showed that a pipeline analog-to-digital converter (ADC) is calibrated with an algorithmic ADC in the background, which is calibrated in the foreground[42]. The calibration overcomes the circuit non-idealities caused by condenser mismatch and finite operational amplifier (opamp) gain in both the ADC pipeline and the ADC algorithm. In RF circuits, digital calibration is also used: for example, Brenna et al. presented calibration techniques that suppress the leakage of the carrier and enable direct conversion architecture to meet WCDMA specifications[43].

Mehta et al., where a closed-loop RF calibration is used in a fully integrated transceiver, including digital MAC layers[6], gives another example. From the transmit mixer output to the receive mixer input, an RF loop-back path is used. A known digital sequence is transmitted and looped back to the receiver during calibration, and the digital signal received is used to correct non-idealities such as DC offset, I / Q mismatch and RF carrier leakage for analog and RF. This relaxes the requirements and saves space and power.

If we observe this trend, then with many calibration points, we can foresee analog circuits. Smart algorithms can find and correct the sources of error in the digital domain. This allows for compensation for at least static errors (gain, mismatch, and even linearity). Because of its wide band nature, noise in the digital domain can not be compensated for: it remains an analog problem. However, detection algorithms can be improved at the system level so that the required bit error rate requires less signal-to-noise. Inductors are used today, for example, in RF circuits to improve the signal-to-noise ratio. If we realize that a few nH inducer; required for the low GHz range occupies the same die area as a simple baseband processor in 65 nm technology, it is clear that smart digital detection techniques can also help to overcome noise problems.

Pure Analog Circuits

The field where the main chunk of signal processing was done was once analogous. A continuous shift to digital signal processing with some analog processing (or conditioning) of the digital core inputs and outputs has been evident since a few decades. In order to get meaningful data into and out of the digital core in an area-efficient and power-efficient way, however, still analog circuits are required. Although the area where pure analog is applied will inevitably shrink to a minimum (non-zero), the analog circuit requirements will continue to increase as the implementation environment for CMOS deteriorates and deteriorates.

The lowering of supply voltage is a fundamental problem for analog CMOS circuits. This issue can be addressed in two ways. Design analog circuits operating at low voltage or designing analog circuits that can withstand higher than nominal voltages of supply.

Over the past 15 years, the first approach has been popular where supply has fallen from 5 V to 1.2 V today. Recently, many new circuit techniques have been developed, such as the switched opamp technique where switches are moved from the signal path to the supply path in the switched capacitor where they need less gate drive[44]. For Gilbert mixer type, a similar approach has recently been demonstrated[45].

Despite all the research effort, today the analog circuit's bare minimum supply seems to be VGS+VDSSAT+v swing, where v swing is the swing of the signal. If sufficient SNR is still needed, the noise must be reduced. The result is that 10 dB less noise will result in 10 times more power consumption (for the same supply voltage, SINAD, bandwidth, etc.).
Even at the cost of power dissipation, thermal noise can be cancelled[46]. 1/f Noise is also a major concern since in a given technology the corner frequency where thermal noise dominates the 1/f noise appears to be proportional to ft. As ft is usually selected high, 1/f noise will also be large to benefit from the bandwidth. For low frequency applications, cutting and double correlated sampling can remove 1/f noise. The technique of switched bias can reduce transistor intrinsic 1/f noise[47].

The second approach is to design circuits higher than nominal voltages of supply. Usually this is done by stacking transistors while taking care not to break down every transistor, including during transients and startup.
These circuits at higher supply were first found in interfacing drivers[37] and later in (RF) PAs[48,49], but nowadays normal "internal" analog circuits also need to use these techniques to achieve current 1 V supply voltage performance. This can be done, but careful simulation must be done by the designers, as moderate breakdown effects are difficult to see during the production test and can occur during the IC's lifetime.

Analog circuits will operate at higher frequencies as well. At high frequencies it’s beneficial to use inductors for high Q circuits, like oscillators and tuned amplifiers Inductor quality factors (Q) increase with frequency and at frequencies beyond say 40 GHz Q factors of integrated spiral inductors are higher than the Q factors of the resonating capacitors. Realizing this, the designer does not have to take care for max Q of inductors, and also since that the values of inductances are small for high frequencies, the inductors can be laid out in a very compact way: for example in a compact U shape instead of a circle[50–54]. So for very high frequencies inductors can be used at many nodes in a circuit.

Wrap Up

For reasons of efficiency (area and power), a lot of functionality has shifted from the (traditional) analog domain to the digital domain over the past decades. There is also a clear trend towards mixing analog and digital in addition to this shift. High-performance digital blocks will include analog sensory and control systems in the near future, while analog circuits tend to include increasing numerical compensation and control.

Table 1: *Control and Function of ICs*

	Controlled:	
	Analog	**Digital**

Function:	**Digital**	Adaptive clock adaptive supply voltage measure temperature measure local various decrease local noise multi-level I/O on-chip modems.	Redundancy parity bit ECC.
	Analogue	Chopping switched circuits switched bias noise cancelling "high-voltage" circuit analog calibration DEM.	Digital calibration pre-distortion post Processing.

CONCLUSIONS

For many years to come, the evolution of CMOS technology will continue, which is beneficial to digital circuits but not analog. This paper provides a comprehensive discussion of relatively new non-ideal effects such as gate-leakage and output conductance, as is a discussion of the likely successor of the conventional MOS transistor.

There have been trends to shift functionalities from analog to digital domains on the basis of system level. And the trend would go on and the domains would go off. The importance of circuit performance for analog and digital control and vice versa will be greater, resulting in a clear trend of each domain.

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