

Neural Networks and Fault Diagnosis in Integrated Analog Circuits

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Abstract

This is a research paper on changing the learning speed of analogue integrated circuits by solving the complications in network scales and diagnosis of circuit faults in neural network and integration with arithmetic mechanisms at a distributed network.

Keywords: Integrated circuits, efficiency, neural network

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INTRODUCTION

With the improvement of science and innovation, blame finding has been given careful consideration, and step by step turn into an exploration hotspot. For electronic circuit blame finding, the exploration of advanced circuit blame analysis has accomplished incredible improvement. Nonetheless, because of component resistances, and additionally with nonlinear circuit and different reasons, the simple circuits blame determination is a great deal more entangled than computerized circuits blame analysis. Along these lines, the exploration of simple circuit blame finding is dependably a hot and testing subject. Numerous specialists have carried on a lot of inquires about, and have introduced numerous determination techniques. At present, the counterfeit neural system innovation is getting to be distinctly develop. This innovation is another answer for simple circuit blame analysis. Contrasted and different techniques, manufactured neural system has great power and solid learning capacity. It can discover laws from substantial information. Neural system innovation has turned into the examination hotspot in the field of simple circuit blame determination. Scientists have exhibited some

determination strategies in view of neural network^[1-8]. In any case, with the expansion of blame modes, preparing tests and tests measurements, the information amount on preparing sets increment enormously. For a general neural system, the preparation effectiveness will decrease^[6-13]. So as to take care of the issues brought about by substantial dataset, another technique for simple circuit blame finding in view of appropriated neural system is introduced in this paper. To begin with, the dispersed neural system model is presented. At that point, the dispersed neural system learning calculation is introduced. Last, the reenactment comes about and the examination investigation are given.

DISTRIBUTED NEURAL NETWORKS

Artificial Neural Networks

Lately, ANNs have gotten awesome consideration in numerous parts of logical research and have been connected effectively in different fields, for example, substance forms, computerized hardware, control frameworks, and so on. ANNs give a component to versatile example characterization. Indeed, even in negative situations, they can at present have hearty

grouping. It ought to be focused on that picking an appropriate ANN design is crucial for the fruitful utilization of ANNs. Every design of ANNs is reasonable for an

extraordinary application and has distinctive exactness contrasted with different models. Figure 1 demonstrates a two-layer organizes^[9–18].

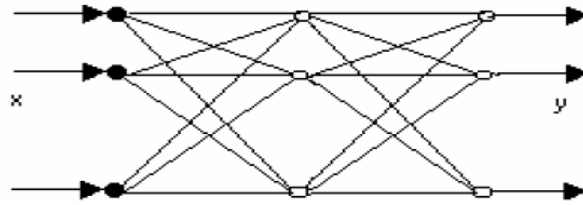


Fig. 1: A Two-Layer Network.

Every information hub is associated with a concealed layer hub and each shrouded hub is associated with a yield hub in comparative way.

Distributed Neural Network Model

Appropriated neural system model is made out of three layers: information layer, dissemination layer and focus layer. The model is appeared in Figure 2. Information layer is made out of an entire preparing dataset. Appropriation layer contains a few

disjoint sub preparing sets and sub neural systems whose information sources are balanced correspondence with the sub-preparing sets. The union of these disjoint subtraining sets is the entire preparing set. In this paper, the sub neural systems are named as dispersion system. Focus layer contains new preparing set which was made by circulation layer and a neural system whose info is the new preparing set. This neural system is named fixation arrange.

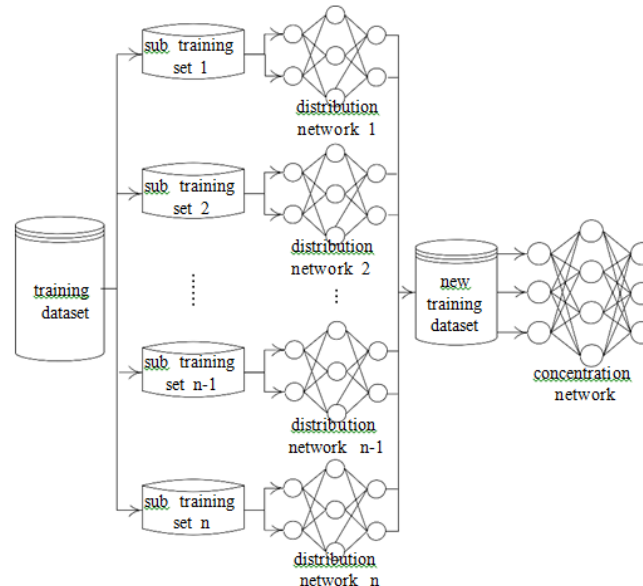


Fig. 2: Distributed Neural Network Model.

DISTRIBUTED NEURAL NETWORK LEARNING ALGORITHM

Algorithm Design

In previous conducted research, a distributed neural network learning algorithm was given. With this calculation, the space limitation issue of

expansive dataset was illuminated, and the learning velocity was moved forward. Utilizing the calculation can bargain adequately with substantial information unsupervised learning issues. But analog circuit fault diagnosis is a typical supervised learning problem because the

fault samples contain not only fault features but also corresponding fault modes.

In this paper, Hebb learning is utilized as learning tenet of dispersion layer in circulated neural system. Then, the class banner is proposed in the calculation. Therefore, the disseminated learning calculation in light of administered Hebb learning standard is proportionate to regularization strategy, the calculation has honesty. Moreover, on the grounds that the class banner was added to the calculation, the learning calculation doesn't dispose of the fractional data because of information part. For the fixation layer of circulated neural system, focus system is a BP neural system. The weight vectors of conveyance systems speak to learning focuses. Another preparation set is shaped by the synaptic weights and the class banners of shrouded

layer neurons in dispersion organize. The new preparing set is utilized as the contributions of the concentrated system. The fixation organize learns by BP calculation^[16-21].

SIMULATION RESULTS AND ANALYSIS

The simulation circuit is shown in Figure 3. This circuit is active band-stop filter circuit. The center frequency of this active band-stop filter circuit is 1 kHz.

$R1=R2=15\text{ k}\Omega$,
 $R3=R7=R9=R10=R11=10\text{ k}\Omega$,
 $R4=6.56\text{ k}\Omega$, $R5=R6=31\text{ k}\Omega$, $R8=5.65\text{ k}\Omega$,
 $R12=1\text{ k}\Omega$, $C1=C2=C3=C4=10\text{ nF}$.

The tolerance of resistances is 5%, and the tolerance of capacitances is also 5%. The unique test point is V_{out} .

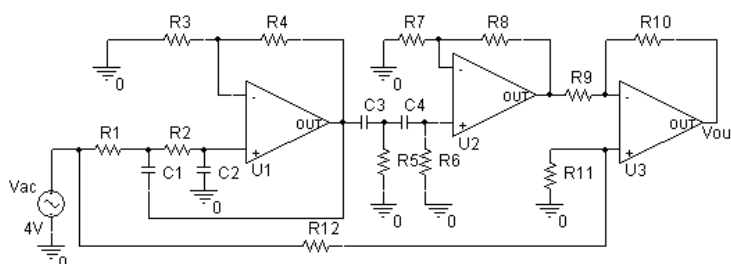


Fig. 3: Active Band-Stop Filter.

The delicate blames because of single resistance or single capacitance are considered. As per affectability examination, the blame modes are set up.

The blame modes are spoken to by "0-1" representation, blame states are spoken to by "0" and typical states are spoken to by "1".

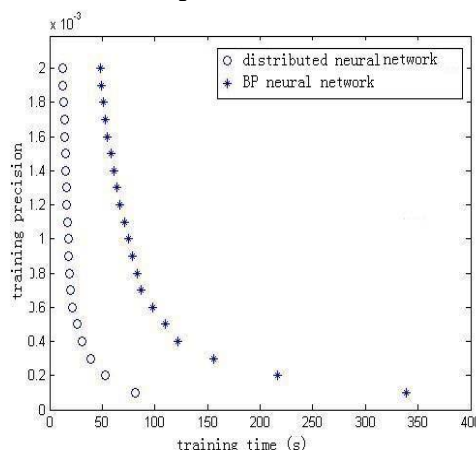


Fig. 4: Relationship between Training Precision and Training Time.

It is shown in Figure 4 that under the same training precision, the training time of distributed neural network which is presented in this paper is always less than the training time of general BP neural network. And it is shown in Figure 5 that the time superiority of distributed neural network increases as the training precision increases.

CONCLUSION

According to the characteristics and the

problems of analog circuit fault diagnosis, a new method of analog circuit fault diagnosis based on distributed neural network is presented in this paper. Simulation results show that the method can solve the problems caused by large dataset effectively, such as the network scale and the training time, etc. The training rate of distributed neural network is more rapid than general BP neural network, and the method is well able to carry out the fault diagnosis.

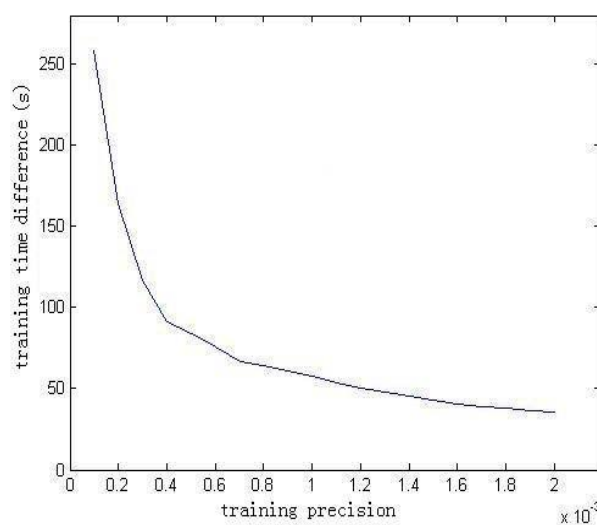


Fig. 5: Relationship between Training Time Difference and Training Time.

REFERENCES

1. Bandler JW, Salama AE. Fault Diagnosis of Analog Circuits [J]. *Proceedings of the IEEE*. 1985; 73(8): 1279–1325p.
2. Walker A, Alexander WE, Lala PK. Fault Diagnosis in Analog Circuits using Element Modulation [J]. *IEEE Des. Test Comput*. 1992; 9(1): 19–29p.
3. Luchetta A, Manetti S, Piccirilli MC. Critical Comparison among Some Analog Fault Diagnosis Procedures based on Symbolic Techniques [C]. *Proc of DATE'02*. 2002; 1105.
4. Peng Minfang, He Yigang, Wang Yaonan. Fault Diagnosis of Analog Circuits Based on Data Fusion for Multiform Circuit Responses [J]. *Journal of Electronic Measurement and Instrument*. 2005; 19(5): 21–24p.
5. Chang YH. Frequency-Domain Grouping Robust Fault Diagnosis for Analog Circuits with Uncertainties. *Int J Circ Theory Appl*. 2002; 30: 65–86p.
6. Worsman M, Wong MWT. Non-Linear Analog Circuit Fault Diagnosis with Large Change Sensitivity. *Int J Circ Theory Appl*. 2000; 28: 281–303p.
7. Catelani M, Fort A. Soft Fault Detection and Isolation in Analog Circuits: Some Results and a Comparison between a Fuzzy Approach and Radial Basis Function Networks [J]. *IEEE Trans. Instrum. Meas*. 2002; 51(2): 196–202p.

8. Mehran Aminian, Farzan Aminian. Neural-Network Based Analog Circuit Fault Diagnosis using Wavelet Transform as Preprocessor [J]. *IEEE Trans. Circuit Syst.* 2000; 47(2): 151–156p.
9. Farzan Aminian, Mehran Aminian. Fault Diagnosis of Analog Circuit Using Bayesian Neural Networks with Wavelet Transform as Preprocessor [J]. *J. Electron. Test.* 2001; 17(1): 29–36p.
10. Aminian F, Aminian M, Collins Jr. HW. Analog Fault Diagnosis of Actual Circuits Using Neural Networks [J]. *IEEE Trans. Instrum. Meas.* 2002; 51(3): 544–550p.
11. Catelani M, Fort A. Fault Diagnosis of Electronic Analog Circuits using a Radial Basis Function Network Classifier [J]. *Measurement.* 2000; 28(3): 147–158p.
12. Catelani M, Gori M. On the Application of Neural Networks to Fault Diagnosis of Electronic Analog Circuits [J]. *Measurement.* 1996; 17(2): 73–80p.
13. Jin Yu, Chen Guangju, Liu Hong. New Method of Analog Circuit Fault Diagnosis [J]. *J. Sci. Instrum.* 2007; 28(10): 1870–1873p.
14. He YG, Tan Y, Sun YC. Wavelet Neural Network Approach for Fault Diagnosis of Analogue Circuits [J]. *IEE Proceedings of Circuits, Device and Systems.* 2004; 151(4): 379–384p.
15. He Jiazhou, Zhou Zhihua, Gao Yang, et al. A Fault Diagnosis model Based On Novel Neural Network Classifier [J]. *Journal of Computer Research and Development.* 2001; 38(1): 93–97p.
16. Wang Junfeng, Zhang Weiqiang, Song Guoxiang. Fault Diagnosis Algorithm of Analog Circuit Based on Multiwavelet Neural Network [J]. *Transactions of China Electrotechnical Society.* 2006; 21(1): 33–36p.
17. Deng Y, He Y, Sun Y. Fault Diagnosis of Analog Circuits with Tolerances Using Artificial Neural Networks [C]. *The 2000 IEEE Asia-Pacific Conference.* 292–295p.
18. Spina R, Upadhyaya S. Linear Circuit Fault Diagnosis Using Neuromorphic Analyzers [J]. *IEEE Trans. Circuit Syst-II: Analog Digit Signal Process.* 1997; 44(3): 188–196p.
19. Sorsa T, Koivo HN. Application of Artificial Neural Networks in Process Fault Diagnosis [J]. *Automatica.* 1993; 29(4): 843–849p.
20. Srinivasan A, Batur C. Hopfield/ART-1 Neural Network-Based Fault Detection and Isolation [J]. *IEEE Trans. Neural Networks.* 1994; 5(6).
21. Barua A, Kabisatpathy P, Sinha S. A Method to Diagnose Faults in Analog Integrated Circuits using Artificial Neural Networks with Pseudorandom Noise as Stimulus [C]. *Proc of 10th IEEE International Conference on Electronics Circuits and Systems (ICECS 2003).* 356–359p.