International Journal of Analog Integrated Circuits
Vol. 1: Issue 1
www.journalspub.com

Symmetrical 7-Level Multilevel Inverter with RV Topology

Amit Khemariya[1], Praveen Bansal[1], Anmol Ratna Saxena[2]*
[1]Department of Electrical Engineering, Madhav Institute of Technology and Science, Gwalior, India
[2]Department of Electrical and Electronics Engineering, National Institute of Technology Delhi, India

Abstract

A multilevel inverter is a power electronic gadget which is fit for giving fancied exchanging voltage level at the yield utilizing numerous lower level DC voltages as an info. Multilevel inverter is broadly utilized for high-control high-voltage applications. It can dispose of the requirement for the progression up transformer and decrease the consonant substance and lower EMI and higher dc interface voltages. In any case, it has a few detriments, for example, expanded number of segments, complex heartbeat width regulation control technique, and voltage-adjusting issue. The consonant substance of the yield voltage waveform diminishes as the quantity of yield voltage increments. This paper gives another topology a switching voltage part to enhance the multilevel execution by remunerating the impediments as specified. The propose topology is actualized in single-stage and three-stage with various heartbeat width balance (PWM) strategies, which requires less number of parts, less bearer flags and entryway drive circuit when contrasted with routine multilevel inverters.

Keywords: multilevel inverter (MLIs), reversing voltage (RV), topology and PWM techniques

***Corresponding Author**
E-mail: khemariyaamit@yahoo.com

INTRODUCTION

Multilevel inverters have strained incredible interest in the power industry. Increasing the number of voltage levels in the inverter without necessitating higher ratings on specific devices can intensification the power rating. A multilevel inverter is a power electronic device that is used for high-power high-voltage applications. Whereas conventional two level inverter have some limitations in high-power high-voltage applications due to switching losses and power ratings.[1,2] There are several advantages to this approach when compared with the conventional power conversion approach: they have higher efficiency because the devices can be switched at a low frequency, power factor is close to unity for multilevel inverters, no EMI problems exist, no charge unbalance problem results when the converters are in either rectification or inversion mode.

An equivalent depiction of one phase leg of inverters with different levels shown in Figure 1, and power semiconductors is represented by an ideal switch with several positions.[3]

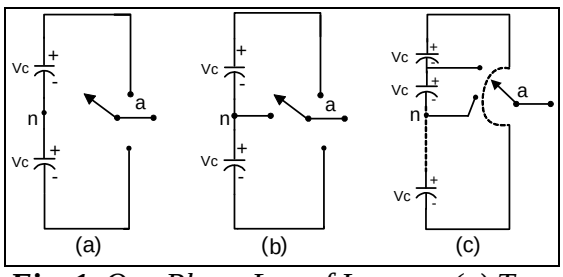
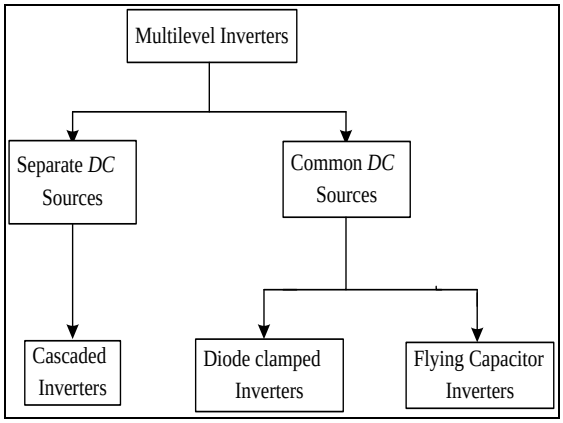


Fig. 1. *One Phase Leg of Inverter (a) Two Level, (b) Three Level, (c) n-Levels.*

Three different major multilevel converter structures have been applied in industrial

applications: cascaded H-bridges (CHBMLI) with separate dc sources, diode clamped (DCMLI), and flying capacitors (FCMLI).



The cascaded H-bridge multilevel inverter or series H-bridge inverter. The series H-bridge inverter appeared in 1975. CHBMLI[4–6] was not completely appreciated until two researchers, Lai and Peng. They original it and obtainable it's various advantages in 1997. The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output.

The output voltage is the addition of the voltage that is produced by each cell. The number of output voltage levels are 2n+1, where n is the number of cells. The control method of cascaded H Bridge multilevel is more convenient than other multilevel inverter because it does not have any clamping diode and flying capacitor. Cascaded multilevel inverter reaches higher reliability. The cascaded inverter is used for large automotive electric drives. However, the requirement of more number of switches and separate dc source for each cell becomes a problem especially at higher level The most commonly used multilevel topology is the diode clamped inverter,[4] in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. It is also called Neutral-Point Clamped Multilevel Inverter. The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter.[7] In general for an N level diode clamped inverter, for each leg 2(N–1) switching devices, (N–1)*(N–2) clamping diodes, (N–1) dc link capacitors and voltage across each capacitor at steady state is V_{dc}/(N–1) are required. In flying capacitor inverter the structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The FCMLI[5] involves series connection of capacitor clamped switching cells. This topology has a step structure of dc side capacitors, where the voltage on every capacitor varies from that of the following capacitor. The voltage augment between two nearby capacitor legs gives the span of the voltage ventures in the yield waveform.

This paper proposes a 7-level multilevel inverter with Reversing Voltage topology which requires less number of switches and gate driver circuits as compared to conventional multilevel inverters. The reversing voltage topology that was previously proposed [8] here is implemented in single-phase and three-phase with different PWM techniques.

PROPOSED TOPOLOGY

This paper presents an overview of a new multilevel inverter topology named reversing voltage. The block diagram of multilevel inverter by reversing voltage topology is shown in Figure 2. In this figure, the left side circuit (i.e., positive level generator) generates the required positive level is called positive level generator and the right side circuit is called full bridge converter which reverses the voltage direction when the voltage polarity requires to be changed for negative

polarity (negative half cycle of the fundamental output voltage).[8]

The main purpose of this paper is to control the EMI, minimize the total harmonic distortion with different PWM techniques using reversing voltage topology and it also minimizes power semiconductor switches than conventional multilevel inverter. For a conventional single-phase 7-level inverter model, it utilizes 12 switches, whereas the proposed model uses only 10 switches.

This proposed RV topology for 7-level MLI requires ten semiconductor switches and three isolated dc sources shown in Figure 2[9,10] which separates output voltage in two parts.

This topology combines the two parts to generate the multilevel output voltage waveform.

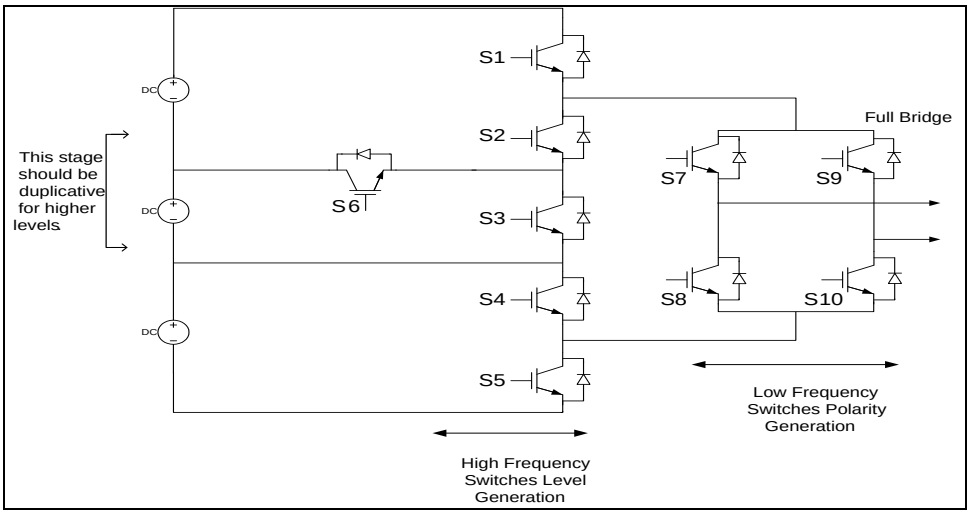


Fig. 2. *Proposed Single-Phase 7-Level MLI Model Using RV Topology.*

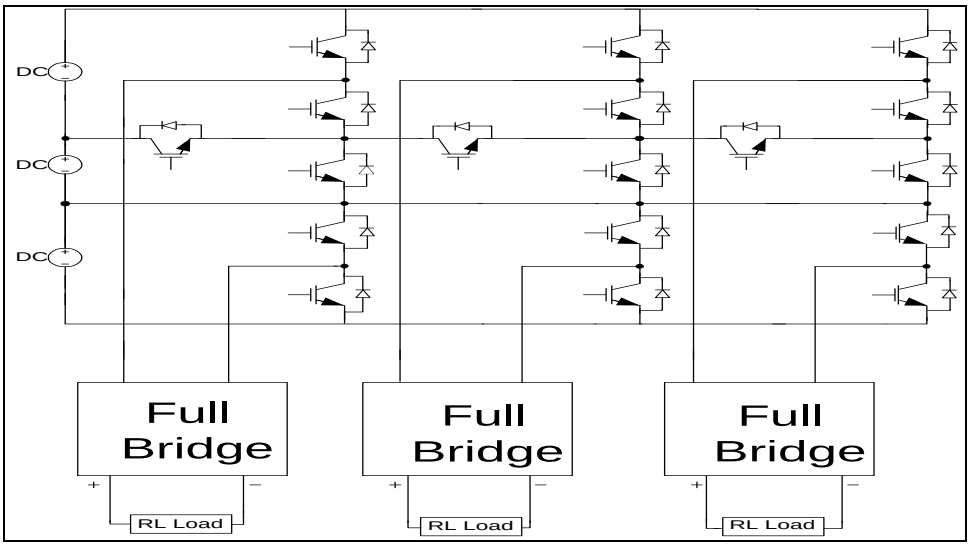


Fig. 3. *Proposed Three-Phase 7-Level MLI Model Using RV Topology.*

The proposed topology is a symmetrical topology because all the values of all voltage sources are equal. This RV multilevel inverter easily extends to higher voltage levels by increasing the middle section as shown in Figure 2. It can also be applied for three-phase applications with the same principle.

Therefore, it does not face voltage-balancing problems due to fixed dc voltage values. In comparison with a cascade topology, it requires just one-third of isolated power supplies used in a cascade-type inverter. [10] In Figure 3, the complete 3-phase MLI for 7-level is shown. For a conventional three-phase 7-level inverter model, it uses 36 switches, whereas the proposed model uses only 30 switches.

The operation of the proposed topology has been discussed in detail and has been verified with the help of simulations. [11]

Table 1. *Operation of A 7-Level Multilevel Inverter Using Reversing Voltage Topology.*

Generation of level	Switching states										Output voltage
	S1	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*	*S9*	*S10*	
3	✓				✓			✓	✓		$3V_{dc}$
2	✓			✓				✓	✓		$2V_{dc}$
1		✓		✓		✓		✓	✓		V_{dc}
0		✓	✓	✓			✓	✓	✓	✓	0
–1		✓		✓		✓	✓			✓	$-V_{dc}$
–2	✓			✓			✓			✓	$-2V_{dc}$
–3	✓				✓		✓			✓	$-3V_{dc}$

Operation of the single-phase 7-level MLI with Reversing Voltage topology can be easily explained with the help of Figure 2 and Table 1. When switches S2, S4, S6, S8 and S9 are turned "on" the output voltage will be "V_{dc}" (i.e., level 1). The output voltage will be "$2V_{dc}$" (i.e., level 2) when switches S1, S4, S8 and S9 are turned "on. When S1, S5, S8 and S9 switches are turned "on" the output voltage will be "$3V_{dc}$" (i.e., level 3). When switches S2, S3, S4, S7, S8, S9 and S10 are turned "on" the output voltage is zero (i.e., level 0). Switches S9, S10, S11 and S12 are used for a complementary pair. When S8 and S9 are turned "on" together, positive half cycle (level +1, level +2, level +3) can be generated and when S7 and S10 are turned "on" together, negative half cycle (level –1, level –2, level –3) can be generated across load. The voltage blocking capacity of each switch is V_{dc}.[2]

MODULATION STRATEGIES

The pulse-width modulation (PWM) control[9] is the most efficient method of controlling output voltage within the inverters. The carrier based PWM schemes used for multilevel inverters is the most efficient method, realized by the intersection of a modulating signal with triangular carrier waveform. The paper tries to prove that RV is better than conventional multilevel inverters in terms of their number of components and THD. There are different pulse width modulation strategies with different phase relationships. Phase disposition pulse width modulation (PD PWM): In phase disposition pulse width modulation strategy, where all the carrier waveforms are in same phase shown in Figure 4.

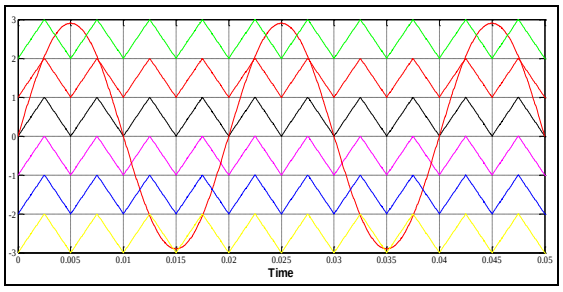


Fig. 4. *Carrier Arrangement for PDPWM Strategy.*

Phase opposition disposition pulse width modulation (POD PWM):- In the phase opposition disposition pulse width modulation strategy, where all carrier

waveforms above zero reference are in phase and below zero reference are 180^0 out of phase. Shown in Figure 5.

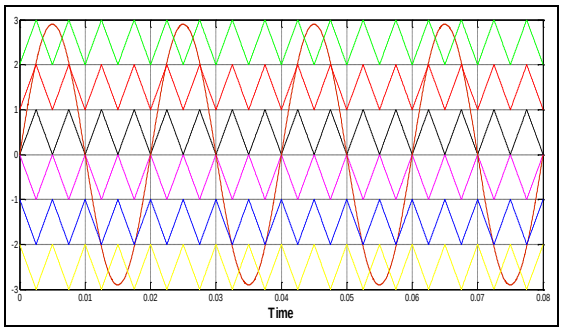


Fig. 5. *Carrier Arrangement for PODPWM Strategy.*

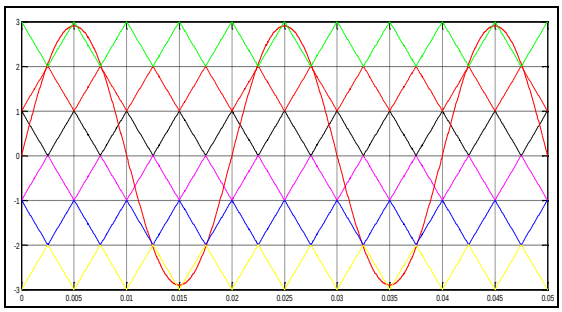


Fig. 6. *Carrier Arrangement for APODPWM Strategy.*

Alternate phase opposition disposition pulse width modulation (APOD PWM): In alternate phase opposition disposition PWM scheme where every carrier waveform is in out of phase with its neighbor carrier by 180°. Shown in Figure 6.

SIMULATION RESULTS

The Figures 2 and 3 show the RV model of single-phase and three-phase 7-level RV MLI. Table 2 shows THD comparison between different PWM techniques. The simulation parameters are as following R = 20 Ohms, L = 10 mH, and dc source voltage is 300 V; frequency of carrier signal is 1 kHz.

In this paper, four PWM techniques are used PD, POD, APOD and corresponding (%) THD are PD =18.62 POD = 18.98, APOD = 18.49, shown in Figures 7–12. Based on the PWM techniques, the harmonic spectrum was analyzed using the FFT Window in MATLAB/Simulink.

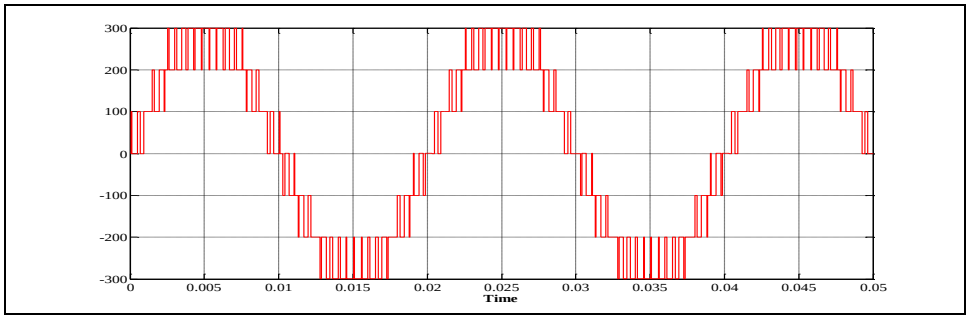


Fig. 7. *Output Voltage Phase a.*

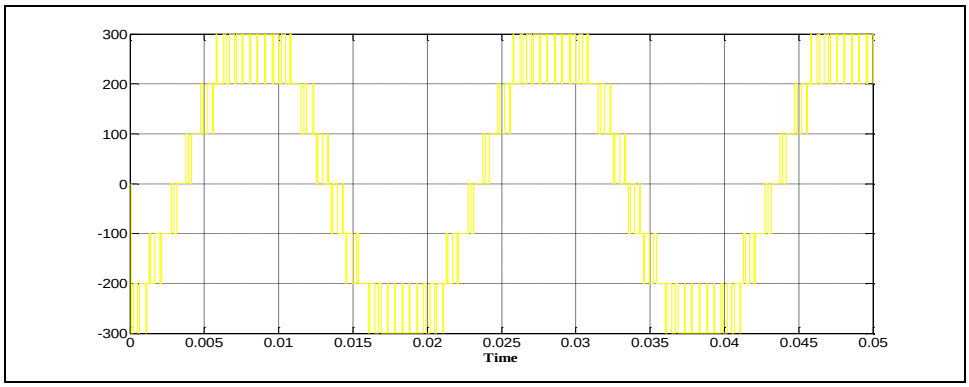


Fig. 8. *Output Voltage Phase b.*

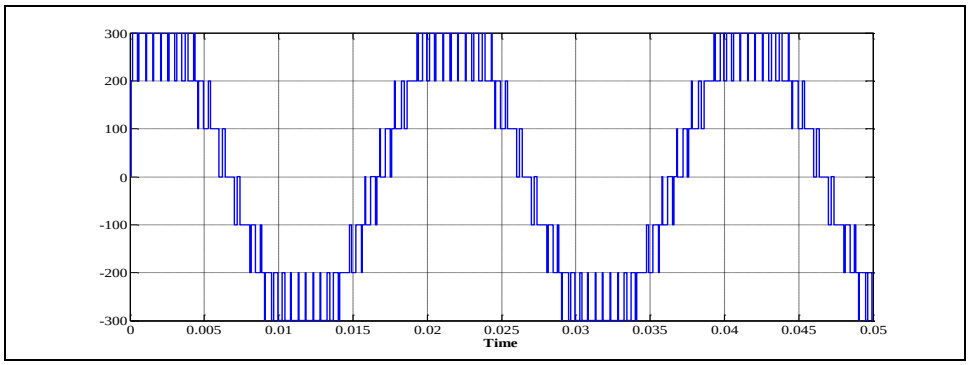


Fig. 9. *Output Voltage Phase c.*

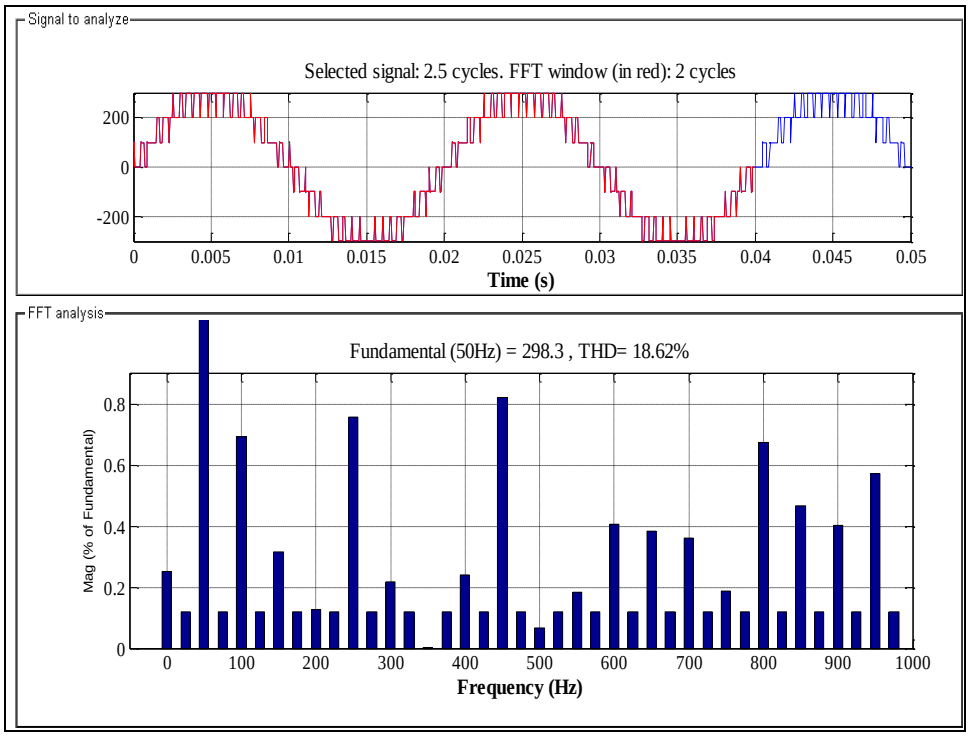


Fig. 10. *Phase Output Voltage by PDPWM for R-L Load.*

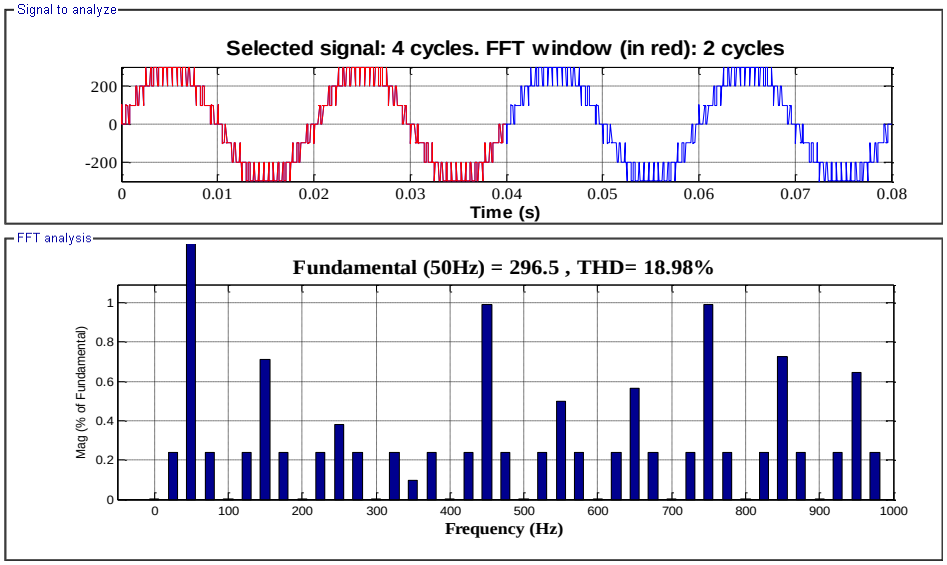


Fig. 11. *Phase Output Voltage by PODPWM for R-L Load.*

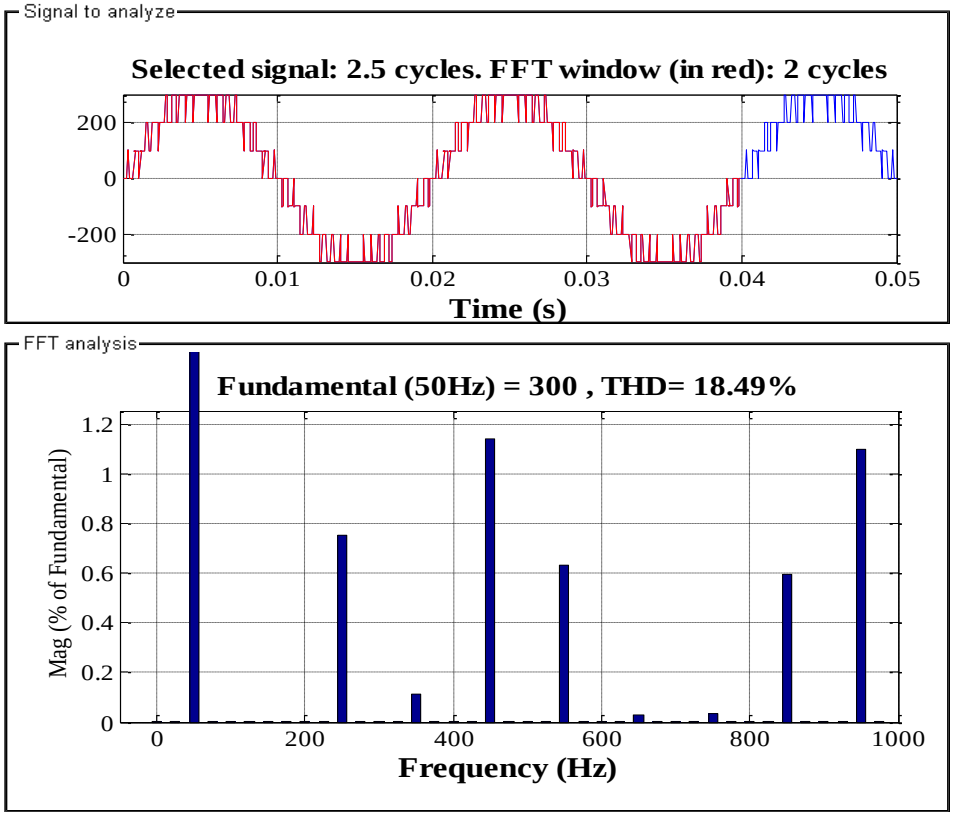


Fig. 12. *Phase Output Voltage by APODPWM for R-L Load.*

Table 2. *THD Analysis b/w Different PWM Techniques for 7-Level MLI.*

Modulation index	POD PWM %THD	PD PWM %THD	APOD PWM %THD
1	18.98	18.62	18.49
0.9	19.48	19.72	19.96
0.8	21.73	22.27	21.91
0.7	21..94	22.86	23.06

The number of required components for three-phase 7-level MLI is shown in Table 3.

Table 3. *Comparison Between Different Multilevel Inverter Topologies.*

Inverter type	NPC	Flying capacitor	CHB	Proposed
Main switches	36	36	36	30
Main diodes	36	36	36	30
Clamping diodes	90	0	0	0
DC bus capacitor isolated supplies	6	6	9	3
Flying capacitors	0	45	0	0

CONCLUSION

In this paper, a 7-level multilevel inverter using reversing voltage topology is proposed with different PWM techniques and used to generate 7-level output phase voltage. It is proved that, the proposed work of Single phase and three phase 7-level MLI output voltage total harmonics distortion is reduced and improve the efficiency of system compare with different conventional topologies of single phase and three-phase 7-level MLI. Harmonic analysis carried out using Matlab R2009a version software. This proposed MLI topology requires less number of components as compared to conventional MLI inverters. Simulation results show the performance of single-phase and three0- phase 7-level MLI with different PWM techniques.

REFERENCES

1. Daher S., Schmid J., Antunes F.L.M. Multilevel inverter topologies for stand-alone PV systems, *IEEE Trans Ind Electron*. 2008; 55(7): 2703–12p.
2. Joshi H., Tekwani P.N., Kolorrol A.H. Multilevel inverter for induction motor drives using RV topology, *IEEE Trans Ind*. 2010.
3. Jang-Hwan K., Sul S.-K., Enjeti P.N. A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage source inverter, *IEEE Trans Ind Appl*. 2008; 44(4): 1239–48p.
4. Yuan X., Barbi I. Fundamentals of a new diode clamping multilevel inverters, *IEEE Trans Power Electron*. 2000; 15(4): 711–8p.
5. Rodriguez J., Lai J.-S., Peng F.Z. Multilevel inverters: a survey of topologies, controls and applications, *IEEE Trans Ind Electron*. 2002; 49(4): 724–38p.
6. Babaei E. Optimal topologies for cascaded sub-multilevel converters, *Power Electron*. 2010; 10(3): 251–61p.
7. Nabe A., Takahashi I., Akagi H. A new neutral point clamped PWM inverter, *IEEE Trans Ind Appl*. 1981; 1A-17: 518–23p.
8. Najafi E., Yatim A.H.M., Samosir A.S. A new topology-reversing voltage (RV) for multi-level inverters, *2nd International Conference on Power and Energy (PECon 08)*. Malaysia, December 2008, 604–8p.
9. Radan A., Shahirinia A.H., Falahi M. Evaluation of carrier based PWM methods for multi-level inverters, *Proc IEEE ISIE*. 2007; 389–94p.
10. Najafi E., Yatim A.H.M. Design and implementation of a new multilevel inverter topology, *IEEE Trans Ind Electron*. 2012; 59(11).
11. Nedumgatt J.J., Vijayakumar D., Kirubakaran A., *et al*. A multilevel inverter with reduced number of switches, *IEEE Students' Conference on Electrical, Electronics and Computer Science*. 2012.